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A new microcontroller-based technique for generating variable voltage/frequency sinusoidal PWM signals

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This paper presents a flexible and robust microcontroller-based technique for generating the control signals of any sinusoidal pulse width modulation (SPWM) scheme for variable voltage/frequency output. The proposed technique exploits the fully static design of a high-speed microcontroller and generates the PWM control signals by varying the controller's clock, while keeping the number of the algorithm processing states constant. As the experimental results show, the technique can be used for transient-free frequency and/or voltage changes with very good resolution and a wide range of applications.

1. Introduction

Reduction of the harmonic content in the output of inverters can be achieved by sinusoidal pulse width modulation (SPWM) in high switching frequencies (Simard *et al.* 1991, Holtz 1994). Various PWM methods have been proposed, but the most widely used are the carrier-based methods, which produce the PWM pulse train by combining a reference sinewave of the desired frequency with a high switching triangular wave, which is called 'the carrier'. The problems encountered in the implementation of these methods are the accurate synchronization of the sinewave with the triangular wave (Yuvarajan and Chiou 1994), and the complexity of the hardware. In analogue-type solutions, the synchronization is achieved by using high-precision components, whereas in microcomputer-based solutions, on-line computation is practical only at low carrier frequency (Johnson 1987), and large memories are required in EPROM-based systems with good dynamic response (Simard *et al.* 1991).

This paper presents a technique for generating SPWM control signals by combining the advantages of EPROM-based and microcomputer-based methods, while achieving accuracy comparable to analogue-based techniques. The technique has been implemented using the MC68HC16Z1 microcontroller of Motorola Inc., but it can be easily implemented using other high-speed fully static designed microcontrollers. The presented technique uses a small look-up table for storing the switching values (expressed in multiples of CPU clock cycles) of the first quadrant of the sinewave, executes the look-up table scanning irrespective of the output frequency and controls the output frequency by modifying the microcontroller's clock, using either an external voltage-controlled oscillator (VCO) or the internal phase-locked loop (PLL). The amplitude is adjusted by determining the modulation depth while scanning the look-up table. Using this technique, large memory requirements are

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eliminated and only two parameters have to be determined in order to change the modulator operational conditions, since the same algorithm, implemented in firmware, is used for any output condition.

2. The generation of SPWM signals

The usual technique for implementing PWM pulses to achieve variable output, either in frequency or voltage, is to use a constant clock for circuit operation with different PWM patterns, or to recalculate the PWM switching points. The presented technique uses a different approach: since the timing characteristics of a state machine depend on its operating clock, different timing relations can be achieved by controlling its clock instead of changing its state diagram. This approach has been used to achieve variable frequency output in the presented PWM modulator. The modulator has been implemented using the MC68HC16Z1 microcontroller, since its fully static design allows variations of its clock without affecting its processing stages.

The MC68HC16Z1 is a high-speed, 16-bit microcontroller, built up from various modules that interface via an intermodule bus, and has been developed for rapid development of specific applications. The microcontroller operates either by using an externally generated clock or by synthesizing its clock from a frequency reference using an internal PLL. Its hardware architecture and software functions support clock changes during operation, due to its static structure (Motorola 1992).

The PWM modulator, built using this microcontroller, uses a small look-up table for determining the PWM switching points, a scanning and processing procedure for implementing the PWM generation state machine and a control module for determining the circuit clock and the output modulation depth. Figure 1 shows the modulator's functional architecture. The PWM look-up table contains the switching points of the first quadrant of a sinewave with frequency equal to the output fundamental frequency f_0. The look-up table contains only one-fourth of the total switching points by exploiting the sinewave symmetry. The output frequency f_0 is equal to $f_c/4c_{pr}k$, where f_c is the clock frequency, c_{pr} is the number of clock cycles needed for each processing state and k is the number of entries in the look-up table. Factor 4 expresses the fact that, for generating a complete sinewave, the PWM look-up table has to be scanned four times, twice in both up and down directions. The look-up table is divided into two parts. The first part contains the duration of each PWM pulse, while the other part contains the time between consecutive pulses. The 'carrier' frequency is f_c/c_{pr} and the first output harmonic is concentrated around this frequency. Using this technique, the 'reference' sinewave and the 'carrier' remain synchronized either in steady-state conditions or in transient periods.

Figure 1 indicates the processing steps performed in each state, most of them implemented in firmware. The system operating conditions (SOC) module processes data from analogue and digital input sources to determine the output frequency and the modulation depth, and uses the internal PLL to set up the clock frequency. A VCO can also be used for external clock generation, but a D/A converter must be connected to an I/O port for digitally controlling the modulator clock. The SOC module also sets the modulation depth parameter and determines the scanning step when the harmonic content has to be limited in a specific frequency area. The SOC is called either at the end of each processing state or at the end of each up/down look-

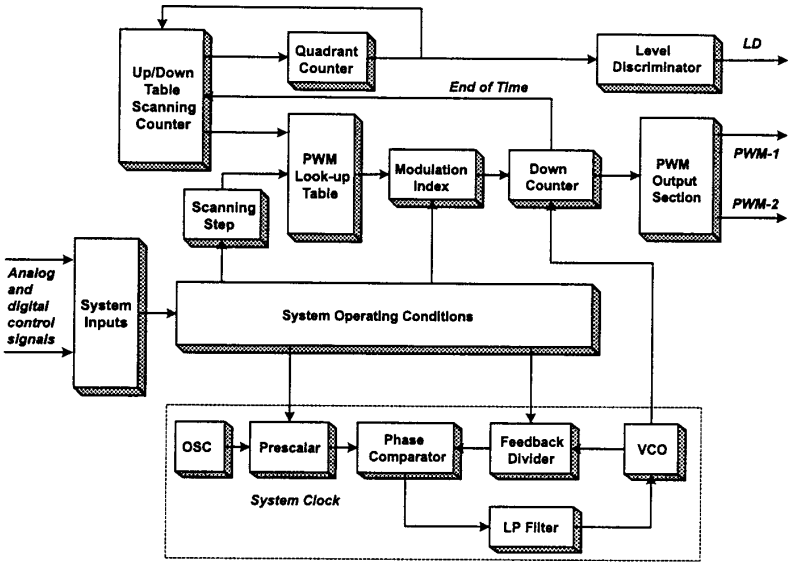


Figure 1. Modulator architecture using the internal PLL-based system clock.

up table scan. In the last case, modifications on the output conditions are applied only when the sinewave crosses zero, thus eliminating any transient phenomena.

Each processing state starts when a PWM output signal is asserted. In this case, the next value of the look-up table is used for determining the PWM signal duration. The look-up table contains the values of modulation depth equal to 1, so the modulation index stage is used for calculating the actual value. The proposed technique is used for implementing high switching frequency sinusoidal PWM (Antonakopoulos *et al.* 1992) that determines the duration of the PWM pulse by the value of the sinewave at the instant of its rising edge. The high switching frequency sinusoidal PWM method uses a sawtooth wave as the carrier and the start of each PWM pulse is at a fixed position. Since the switching ratio (carrier frequency/modulating frequency) is very high, the modulation index (m) is related to the pulse duration (t_k) by the equation

$$t_k = m\frac{1}{f}\left|\sin\left(\frac{\pi}{N}(k-1)\right)\right|$$

where f is the carrier frequency and $2N$ is the number of pulses generated during a sinewave period. Therefore, the duration of each pulse is determined by multiplying the respective look-up table value by the modulation depth.

The down counter has been implemented by a software routine, while the modulation index output and the system clock determine its execution time. The two PWM outputs are fired alternately for generating complementary pulse trains. When the down counter finishes its execution, it passes the CPU control to the table scanning counter (TSC), which reads the next look-up table entry to determine how long both PWM outputs have to remain unasserted. When the time expires, the system enters the next processing state. Dead times for avoiding simultaneous

conduction of power section transistors are included in this part of the look-up table. Figure 2 shows an example of the two PWM pulse trains, which correspond to the intersection of the sinewave with the reference sawtooth signal. Due to the high switching frequency, it can be considered without introducing noticeable errors that during each sawtooth interval the sinewave maintains its amplitude.

Each time the TSC pointer reaches one of its boundaries (0 or $k-1$), the value of the 2-bit quadrant counter (QC) is increased and the TSC changes its mode of operation (from upward to downward and vice versa). If the QC output is 0 or 1, the level discriminator output is 'low', indicating that the generation of the first half-cycle is in progress, whereas if the QC output is 2 or 3, the level discriminator output is 'high', indicating the second half-cycle. The output signal of the level discriminator module is used to discriminate the half-cycles in the power section. When the output of the level discriminator is at a low level, the generated sinewave at the power section has positive values, wheras a high level at that signal forces the power section to generate the negative values half-period of the sinewave (Antonakopoulos *et al.* 1992).

By estimating the maximum number of clock cycles required for each processing stage, the firmware is organized so that the number of clock cycles required for each processing state is constant and independent of the operating conditions. Although the technique presented here has been used for open-loop PWM signals generation, it can be extended for closed-loop configurations by incorporating in the processing steps the on-chip A/D converter channels for sensing the line conditions.

Using the internally generated clock, the modulator dynamic range is given by the following equation

$$F_m \cdot \frac{p_{min}}{p_{max}} \leq f_0 \leq F_m$$

where F_m is the maximum output frequency, p_{min} and p_{max} are the maximum and minimum clock prescaler values. Experimental results show that the p_{min}/p_{max} ratio can take values less than 0.1, depending on program memory characteristics. Furthermore, the frequency resolution varies from 1.56% to 3%, since the micro-

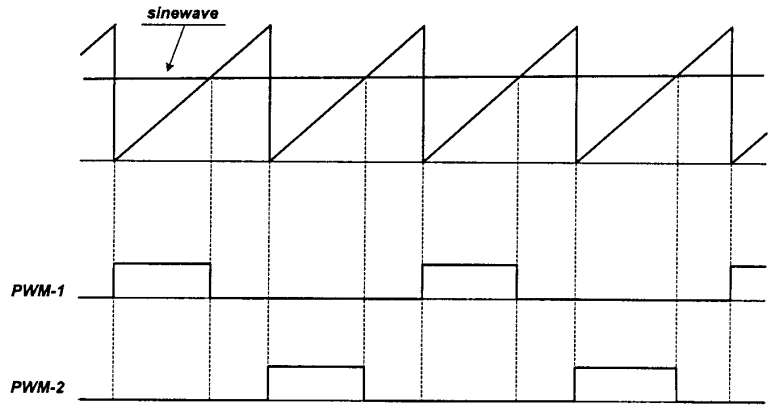


Figure 2. The PWM pulses generation process.

controller prescaler has better accuracy at the lower part of its dynamic region. The use of an external clock generator gives more accurate performance, although it increases the hardware complexity. By using an 8-bit D/A converter for VCO driving, 0.4% accuracy can be achieved, while by using a 10-bit D/A converter the accuracy is increased to 0.1%.

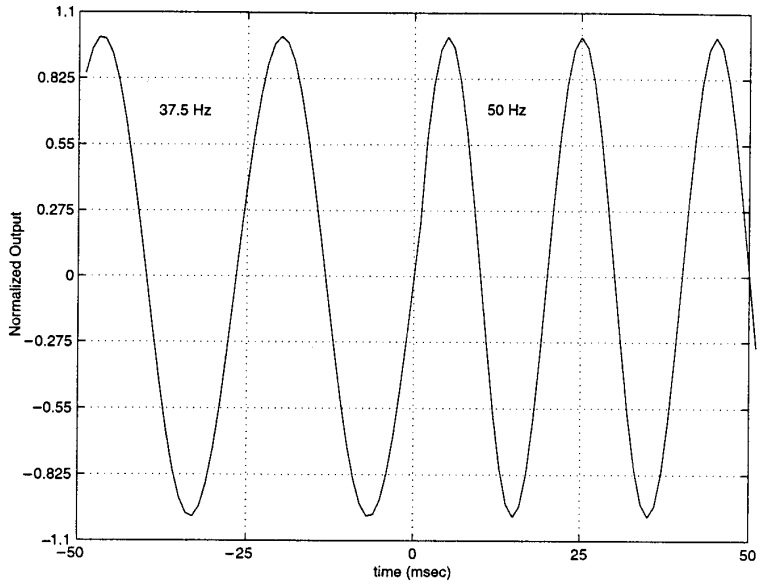
The M68HC16 family also has some members with flash EEPROM modules (FEM) with independently erasable blocks, like the MC68HC916X1. These modules can be used for reconfiguring the controller contents during operation. The first FEM module can be used for downloading purposes, while the other FEM module can be used for storing the look-up tables and the scanning algorithm. When new data have to be downloaded in the microcontroller, the generation of SPWM signals is suspended, the clock takes its default value and the program control is transferred to the downloading control module. Then the second FEM module is bulk erased, new data—look-up table and processing algorithm—are loaded and the new modulator is activated.

The technique described in this paper can be easily extended to 3-phase PWM inverters for electrical drive systems. In that case some modules have to be used three times, while other modules are used once. The system look-up table, the SOC module, the clock generation section and the I/O interfaces remain the same as in the single-phase system. The modules, which are related to the generation of the PWM pulse trains, are used in triplicate, one module per phase. The 120° angle difference is achieved by using different initial values of the table scanning counter during system initialization.

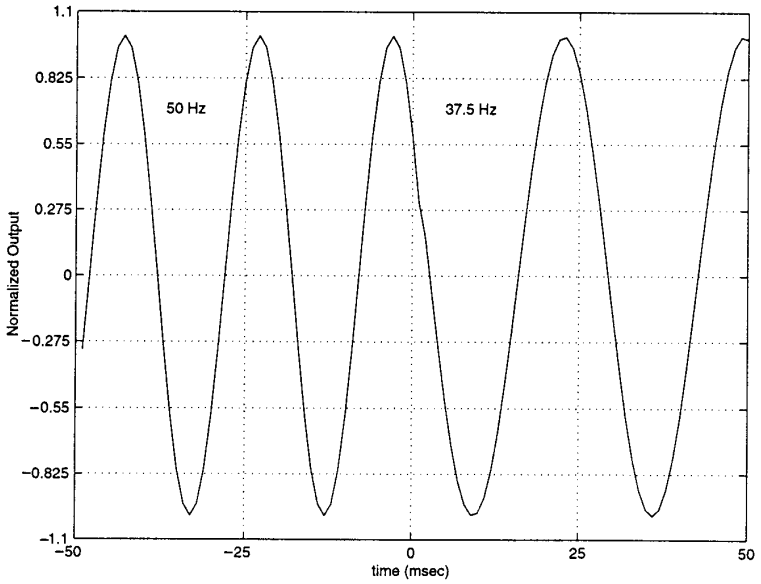
3. Experimental results

The proposed technique has been implemented using the MC68HC16Z1EVB evaluation board of Motorola Inc. (1992) using either the internally generated clock or an external clock. Figure 3 shows the response of the sinewave generator. Three different cases are shown: frequency control keeping voltage constant, voltage control keeping frequency constant, and simultaneous voltage and frequency control keeping voltage/frequency (V/f) constant. In all cases, upward and downward conversions are shown, using the internally controlled clock, while the modulator operating parameters are determined by an external analogue signal. Due to the high 'carrier' frequency and in order to present the modulator performance in transient periods, the PWM pulse trains have been passed through a low-pass filter having its −3 db point at 2.5 kHz. In the experimental results, 50 Hz (prescaler value = 320) and 37.5 Hz (prescaler value = 240) frequencies have been used, and modulation indexes of 0.625 and 0.469. In all cases the parameter k is equal to 65, while the 'carrier' frequency is 13 kHz and 9.75 kHz respectively. Since two bytes are used for each switching point, the look-up table requires 260 bytes in total.

Figure 4 presents the behaviour of the MC68HC16Z1 internal clock circuit during system clock changes from 10.485 MHz to 7.864 MHz and vice versa. The resynchronization time is less than 1 ms, either in upward or downward frequency conversion. Although the processor specifications determine 20 ms as the maximum clock resynchronization time, experimental results show that, at room temperature, this time varies from 1 ms to 3 ms, depending on the changes of the clock frequency. The microcontroller operates in the range of 131 kHz up to 16.78 MHz with the on-chip PLL, but the experimental results show that, by using the MC68HC16Z1EVB

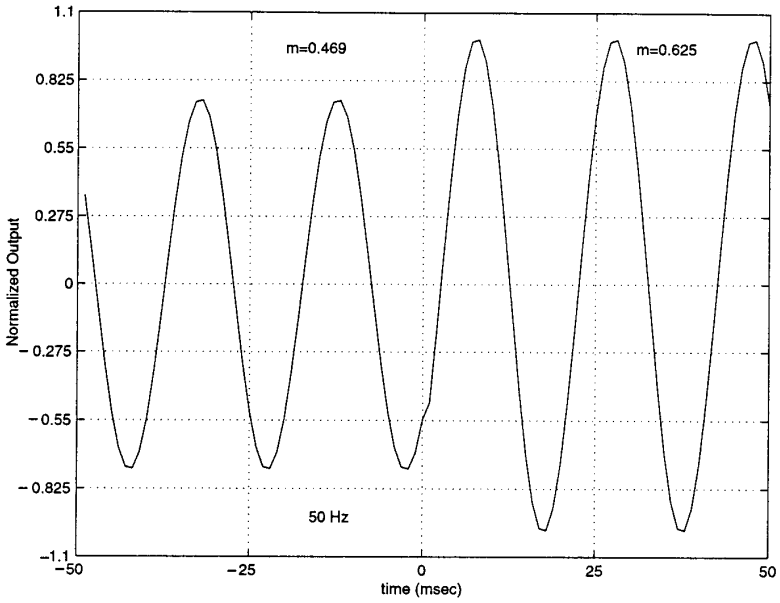


(*a*)

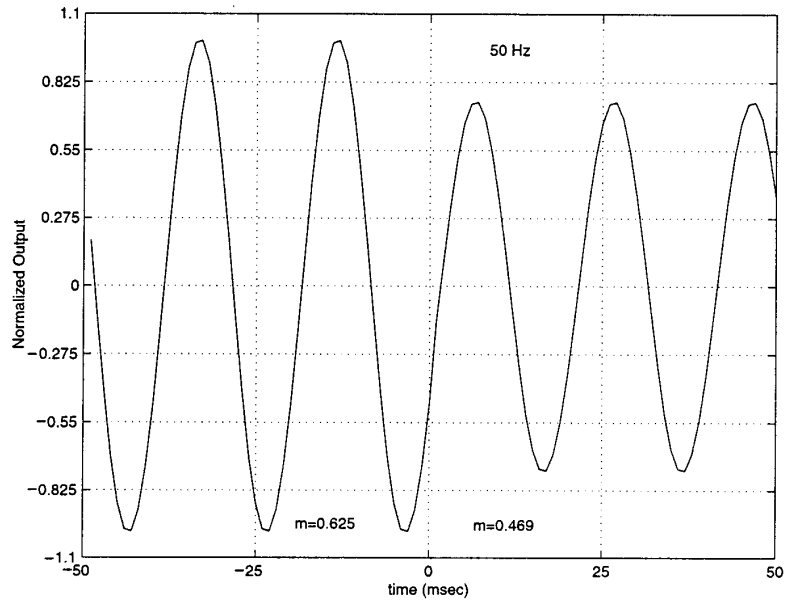


(*b*)

Figure 3. Modulator performance in changing upward and downward parameters: (*a*), (*b*) varying the output frequency; (*c*), (*d*) varying the output amplitude; (*e*), (*f*) keeping the amplitude/frequency ratio constant.

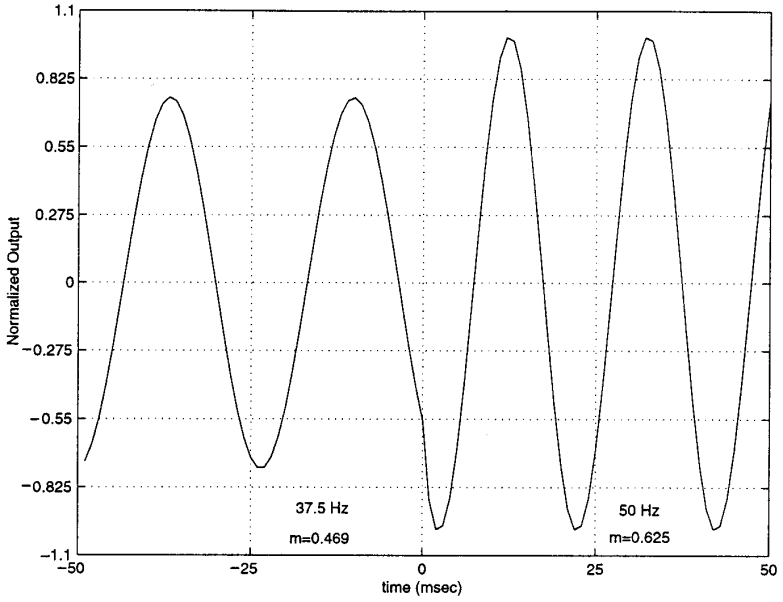


(*c*)

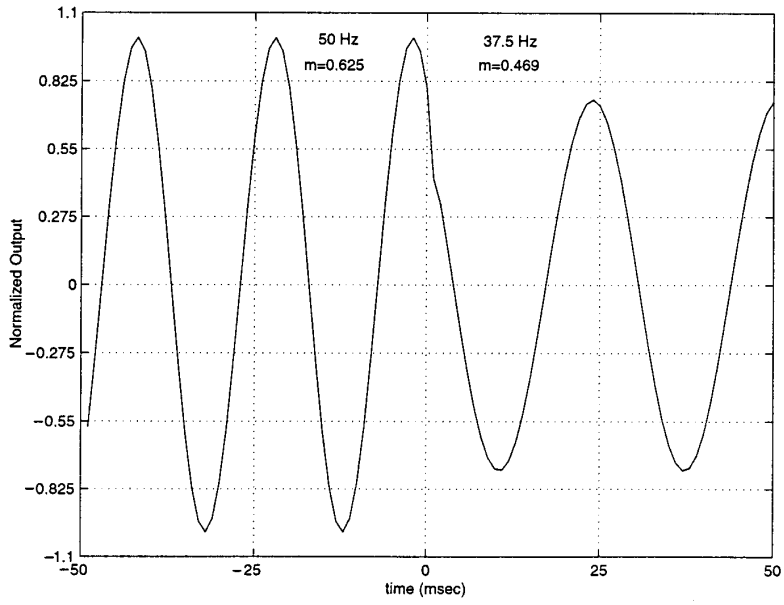


(*d*)

Figure 3. (*continued*)



(*e*)



(*f*)

Figure 3. (*continued*)

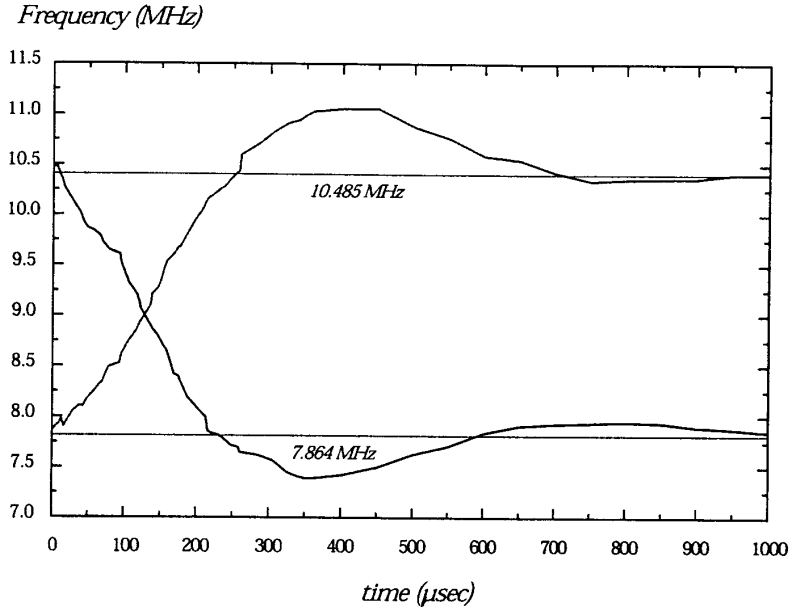


Figure 4. Clock synchronization time from 10.485 MHz to 7.864 MHz.

board, stable operation during frequency change is achieved in the range of 2.097 MHz up to 16.777 MHz, due to hardware limitations. This results in a dynamic range of the experimental prototype of 3 octaves.

4. Conclusion

This paper presents a simple, accurate and easily reconfigurable technique for variable frequency SPWM control of signals generation by using a microcontroller with variable clock speed. The modulator can easily modify its output characteristics without changing its processing procedure by setting up the modulation depth and the operating clock frequency. Because the processing procedures are independent of the output frequency, no synchronization problems are encountered. Application-dependent accuracy and dynamic range can be selected by using either an internal PLL (1.56–3%) or an external programmable clock generator (0.1% using a 10-bits A/D).

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