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V-NET: An Adapter Card for Wireless Local Area Networks

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Abstract. The key aspect of the revolution on the telecommunications is the ubiquitous access to information and services anywhere and at anytime. Wireless communications give a new meaning to the concept of ubiquitous access. Cellular service combined with the POTS network gives this capability to telephony. However, in packet networks there is still a long way to go. IEEE 802.11 was accepted as a standard last summer, and interoperability tests are planned only for the future. The business focus of DCT Hellas is on data communication systems including wireless, wireline and optical communications. Within the framework of OMI[†], DCT Hellas is developing a MAC controller based on the ARM core CPU, which is integrated with additional on-chip logic to provide the interfaces with the PCMCIA bus and an RF transceiver at the ISM band using Direct Sequence Spread Spectrum transmission. DCT Hellas is also developing the microcode to implement the IEEE 802.11 standard. The architecture of this system is presented in this paper.

Index Terms. Wireless Communications, ARM, ASIC design, IEEE 802.11, ISM.

1. Introduction

The IEEE 802.11 standard for Wireless LANs (WLANs) [1] is a significant milestone in the evolution of wireless networking technology. The standard is limited in scope to the physical (PHY) and Medium Access Control (MAC) network layers of the OSI model. It specifies a choice of three different PHY layers, any of which can underline a single MAC layer. Specifically, the standard provides for an optical-based PHY that uses infrared light to transmit data, and two RF-based PHYs that uses different types of spread spectrum radio communications (FHSS and DSSS). FHSS systems use conventional narrow-band data transmission techniques but regularly change the frequency at which they transmit. The systems hop at a fixed type interval around a spread band using different center frequencies in a predetermined sequence. The hopping phenomena allow the FHSS system to avoid narrow-band noise in portions of the transmission band. DSSS systems artificially broaden the bandwidth needed to transmit a signal by modulating the data stream with a spreading code. The receiver can recover the originally transmitted data even if noise persists in portions of the transmission band. In 802.11, the DSSS PHY defines both 1 and 2 Mbps peak data rates, using Differential Binary Phase Shift Keying (DBPSK) and Differential Quadrature Phase Shift Keying (DQPSK).

This paper focuses especially on the design approach adopted for developing an ASIC which implements the functionality of 802.11 MAC Layer. The final system integration is also presented. Emphasis has been given to the flexibility of the chip architecture, which was imperative due to the demanding nature of 802.11 standard. Furthermore, we had to deal with the incompatibility among similar devices in nowadays market, which are more or less application specific, deviating from the strict line of 802.11 specifications. The above prerequisites were the motive for the development of a programmable communication processor, capable of executing all the mandatory and many optional functions of 802.11 protocol and coping with interoperability problems with existing wireless adapters based on this technology, due to its reconfigurability.

The very recent release of the 802.11 protocol and the lack of testing tools for 802.11 MAC implementations leaded us to the development of an emulator board, in order to validate the protocol functions before the whole design become an ASIC. This strategy gave us the opportunity to use this emulator as a demonstrator of a wireless LAN before the fabrication of the ASIC. The demonstrator includes the Radio Frequency (RF) front end, the Baseband Processor, the Medium Access Controller, and a PCMCIA interface. The adapter operates in the Industrial, Scientific and Medical (ISM) band at 2.4 GHz using Direct Sequence Spread Spectrum (DSSS) transmission. It is implemented using off-the-shelf components with the exception of the MAC Controller, which is configured using the ARM core CPU integrated with additional on-chip logic to provide for a suitable part for this application. The microcode of the IEEE 802.11 protocol is implemented to run on this MAC Controller.

While IEEE802.11 offers aggregate throughput comparable to that of 10-Mbps wired Ethernet, some applications such as multimedia demand higher peak data rates. Moreover, these rates will allow more nodes to be effectively connected to a WLAN via a single channel. The next step in the evolution of 802.11 is most likely a standard for higher data rates, expected in the 10 Mbps and above range. In an IEEE meeting, a draft Project Authorization Request (PAR) was prepared for 20 Mbit/s in the 5.2 GHz band.

The V-Net project is executed in the framework of the Open Microprocessor Initiative (OMI). This project is both timely and viable towards the objectives of the OMI program. By integrating a CPU core with application firmware within the OMI environment, the project team demonstrates the product development benefits advocated by the OMI process and provides constructive user feedback to OMI technology developers. The experience gained from carrying out that implementation can be used to provide promotion of best practice, training, and support services to other SMEs in Greece interested in participating in the application of the OMI concept in their product design. This is in concert with the OMI User Support Network initiative and can facilitate the stimulation of SME interest in Greece in the results that can be achieved through the use of OMI technology and design practice.

The architecture of a system that can be used for the implementation of the wireless MAC protocol is presented in the second chapter of this paper. A block level description of the emulator board is given in Section 3, presenting the system functionality. This is also the internal structure of the ASIC. Finally, Section 4 presents the work that is in progress and the technology trends.

2. Architecture of a Wireless MAC protocol

Cellular services combined with POTS networks give the capability of ubiquitous access to telephony. However, in packet networks there is still a long way to go to fulfill this goal. The IEEE 802.11 wireless MAC protocol is a recent standard which aims to give guidelines

to vendors who are involved in implementations of wireless products. DCT Hellas is working on the development of a PCMCIA board, which will be used mainly to replace wired network cards, in order to give more flexibility to the user. All the available implementations in the market of the IEEE 802.11 MAC layer could only fulfill a subset of the protocol requirements, so the implementation of a new MAC which will be fully compatible with the IEEE specs was decided. A powerful processor core with the necessary additional logic to implement the interfaces with the peripherals should be designed. A module implementing the functions of the PHY layer conforming to the requirements of the IEEE 802.11 standard was the PRISM chipset from Harris Semiconductor [2]. The ARM core, a 32bit RISC CPU, was chosen for the heart of the system. All the necessary modules of the IEEE 802.11 MAC are shown in the block diagram of Figure 1. In this figure, all modules with gray background have been implemented from DCT Hellas using Verilog. To test this code an emulator board, which is presented in the next chapter, was developed.

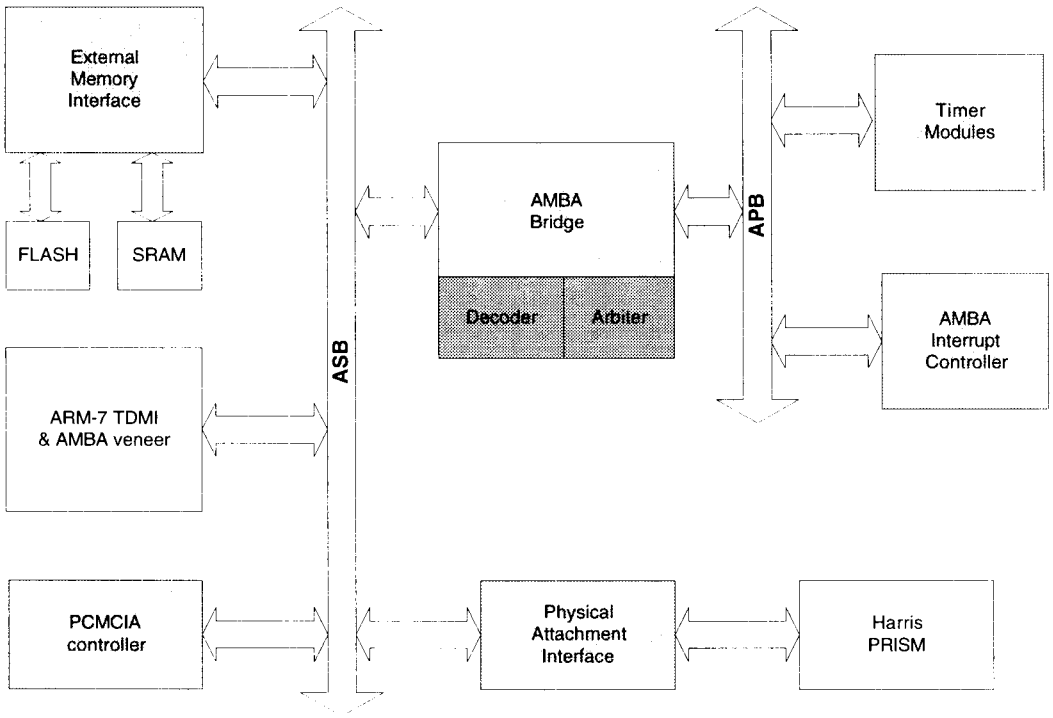

Figure 1. VNet Block Diagram

As illustrated in the above figure the major functional blocks of the VNet architecture are the following:

- ARM-7/TDMI core with the AMBA veneer. The ARM core implements all the MAC functions such as, frame formatting, DCF, Fragmentation, Reassembly, RTS/ACK/CTS etc. through firmware. ARM-7/TDMI core can support two alternative instruction sets [3]: (a) a powerful 32-bit instruction set (when in ARM mode) for implementation targeting to high speed, and (b) a 16-bit instruction subset for more compact implementations. The AMBA Veneer turns the ARM core into an AMBA bus master according to the AMBA specifications [4].
- The PCMCIA module, which performs all the necessary functions for communicating with the host. The PCMCIA module is also implemented as an AMBA bus master, in order to give to the host the capability to access the VNet memory space. It also contains all the appropriate logic to implement the PCMCIA 2.1/JEIDA 4.2 compatible plug and play standard [5].

- The External Memory Interface controller, performs all the necessary functions for interfacing with external memory devices, and supports all the transfer modes (byte, half-word and word access) of the ARM core. It is implemented as an AMBA bus slave module.
- The Decoder module decodes the appropriate slave module that should respond to a master's request. It uses an independent select signal for each slave module.
- The Arbiter module selects the master device that should drive the AMBA bus. The Arbiter module implements a simple priority scheme, where the PAI has the highest priority and the ARM is the lowest. The arbiter module uses 2 signals for each bus master that are used to implement the master state machine.
- The AMBA bridge module contains all the glue logic for connecting slow peripherals on the AMBA bus. It works with 1/3 of the speed of AMBA bus and generates all the necessary peripheral bus signals according to advanced peripheral bus (APB) specifications.
- The AMBA interrupt controller drives the FIQ (fast interrupt request) and IRQ (interrupt request) signals of the ARM core. It accepts all interrupt request signals from the rest of the modules and selects the appropriate interrupt line according to a fixed priority scheme. The IC is implemented as an APB peripheral.
- The AMBA timers module is used for MAC specific functions that require accurate time calculations. It contains two 32-bit counters with independent programmable prescaling, that can count with up to 50 nsec accuracy.
- The Physical Attachment Interface PAI module. This module performs all the necessary functions for interfacing with Wireless PHYs. A detailed diagram of the PAI module is illustrated in Figure 2.

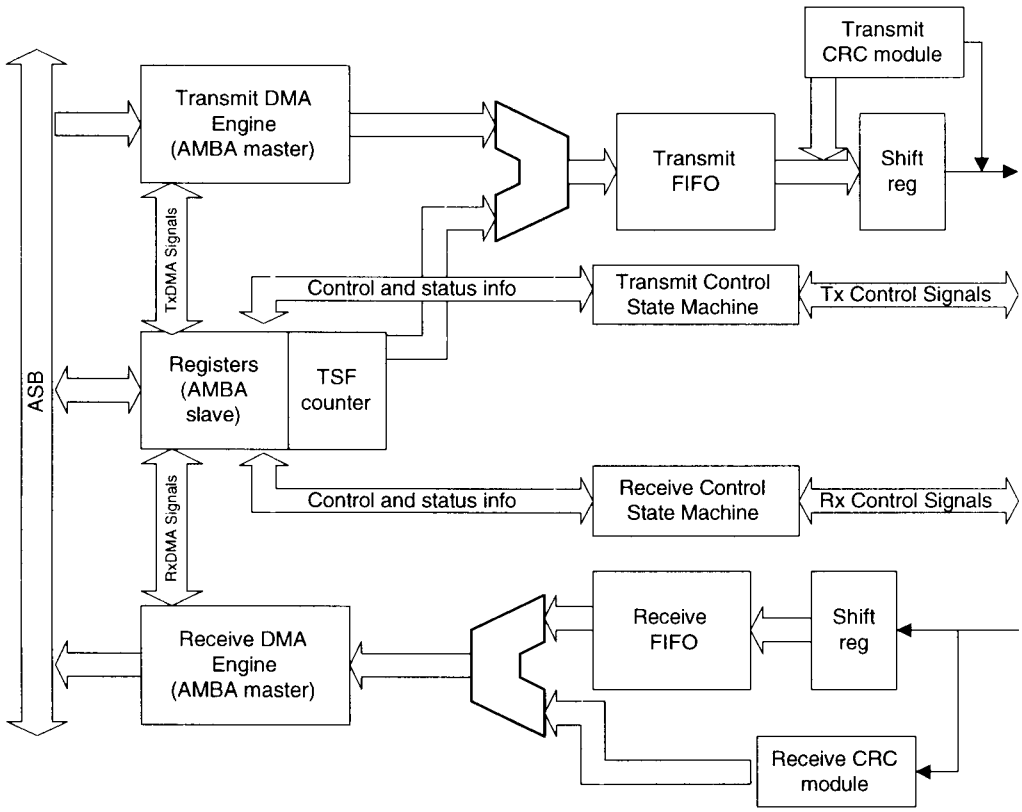

Figure 2: The Physical Attachment Interface.

The PAI module consists of the following blocks:

- The Transmit and Receive control state machines that control all the blocks of the PAI according to the configuration information contained in the AMBA registers and the control information coming from the network.
- The Transmit and Receive DMA machines which perform data transfers to and from the memory independently of the processor, hence, they incorporate bus master logic,
- The AMBA slave registers that store all the control/status information coming from the firmware and the control state machines,
- The 64-bit Time Synchronization Function (TSF) counter which can be configured to count according to a programmable pre-scaler, and provides all the timing information required be WLAN protocols,
- The Receive and Transmit FIFOs which temporally store the bytes received from the network or are prepared for transmission into the network,
- The CRC-32 engines for receiving and transmitting, and the serial to parallel shift registers.

The PAI module can be configured to automatically handle many time-critical physical network management tasks and to provide primitives for efficient WLAN MAC protocol implementation.

3. The Emulator board

The V-Net project aims at developing both technology and products by applying that technology. The technology comprises the communication processor, software routines that implement the WLAN protocol and general purpose routines for handling various peripheral subsystems within the communication processor. Because of the need to speed-up the microcode development cycle, to debug most of the custom hardware functions, and to perform interoperability tests, even before having the real hardware, an emulator board based on an ARM CPU and multiple Field Programmable Gate Arrays (FPGAs) was designed. Actually, this is an application independent board for rapid prototyping of custom ASICs based on the ARM CPU core. The board allows firmware development and in-circuit emulation of embedded systems before having the actual IC.

The V-Net Emulator Board (VEMUL) illustrated in Figure 3, has been developed, in order to prove the functionality of the architecture described in the previous section in hardware. The Emulator board consists of:

- An ARM daughter-board which contains the ARM core, the AMBA veneer and all the necessary logic to interface to the ARM development software through Embedded ICE interface, which provides communication between Embedded ICE macrocell (contained in ARM core) and the host computer,
- Six Xilinx FPGAs for implementing the architectural blocks described in the previous section,
- a PCMCIA extender that interfaces with the Harris PRISM chipset, and
- SRAM and Flash memory modules for firmware storage and development.

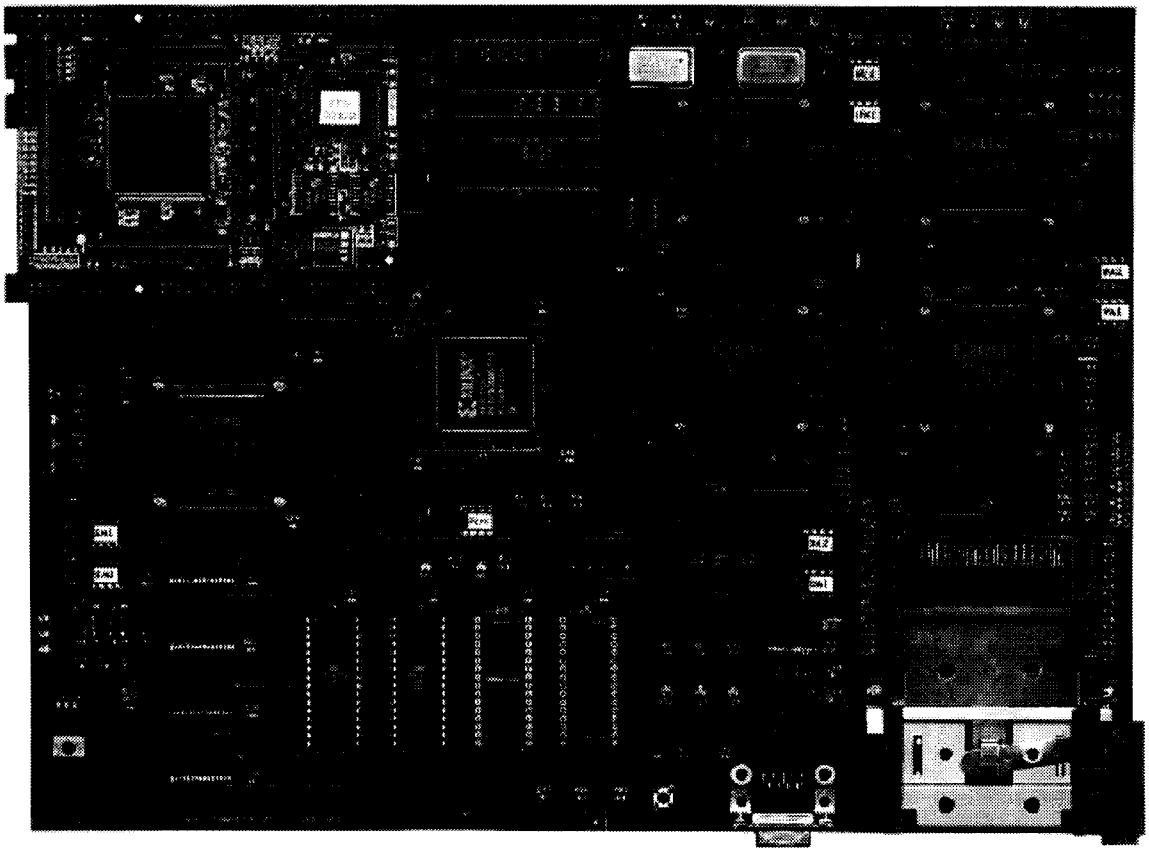

Figure 3: The Emulator Board.

The Emulator board was extensively tested and proved to be fully functional. The testing procedure completed in 3 steps. In the first step the low level hardware functions were tested using firmware code. In the second step, the whole system was tested for transmit and receive directions using a VNET traffic analyzer called VANAL which was also developed from DCT Hellas. In the final step we implemented a wireless link between two emulator boards connected at different PCs as illustrated in Figure 4.

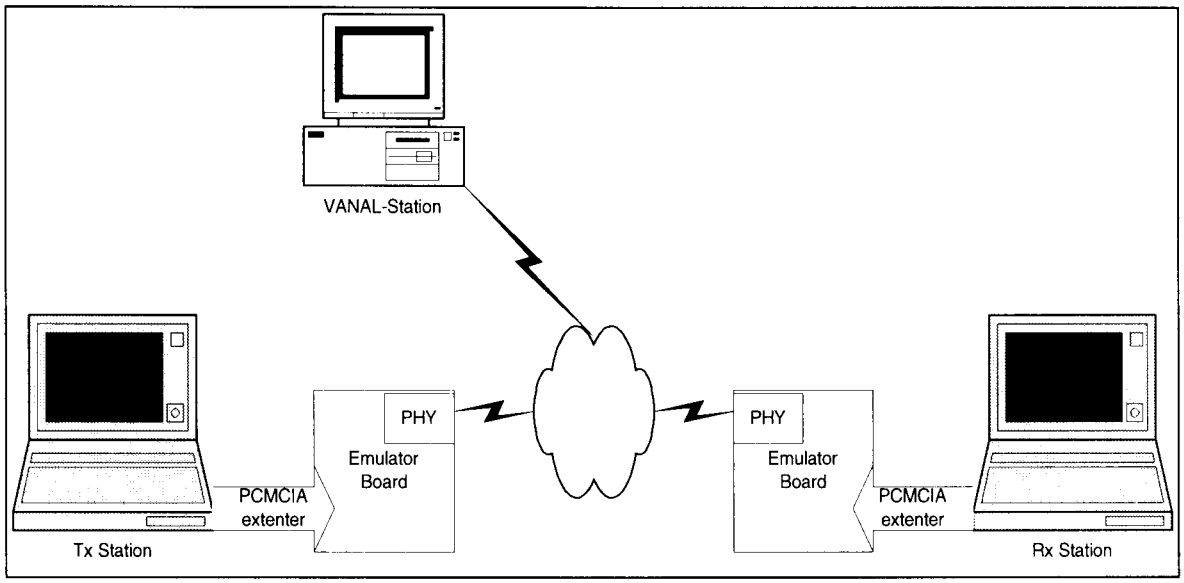

Figure 4: The testing environment

The VEMUL board can be used for the development and testing of other systems based on the ARM core, due to its re-programmable logic. Modules of the VNet system like the external memory controller and the PCMCIA interface could be used without any changes. The external memory controller for instance, is implemented in one FPGA and the code is available in Verilog. The Verilog code for the PCMCIA module, following the PCMCIA 2.1/JEITA 4.2 compatible plug and play standard is also available and can be loaded into another FPGA. This module can be replaced by any other module implementing the interface with any other bus such as ISA or PCI as the FPGA can be reconfigured to control any bus through the flat cable connectors which exist on the board and the respective bus extender. Finally, four FPGAs can be used to develop code to control any local PCMCIA board, by using the PCMCIA socket that exists on the board. These FPGAs, can also be used for the development and testing of any standalone system having any functionality. A serial port and a connector for an LCD, exists on the board to give more options to the designer.

4. Conclusions

The implementation of the IEEE 802.11 MAC is just a part of the whole system, where wireless stations communicate with other wireless or wired stations. In the short term DCT Hellas plans to make a revision of the chip on which the optional Wired Equivalent Privacy (WEP) algorithm and Power management will be implemented. DCT Hellas has also developed an IEEE 802.11 protocol analyzer to be able to monitor the traffic and check the conformance of the traffic with the standard.

The benefits gained from this work are related with two different products: first, the ASIC which implements the 802.11 MAC functionality can be considered as innovative product in the area of wireless communication since it can be appropriately programmed to execute a subset or all of the defined 802.11 functions and remotely communicate with existing devices which are not necessarily 802.11 compliant. The other product that can be used in future projects related to wireless communication, is the emulator board which is based on a high performance CPU and the concept of a common bus shared among a number of peripherals. This can be considered as a multitask system where each peripheral implements a task, resulting to the release of the CPU from time consuming functions. The functionality of each peripheral can be varied according to the specific application since FPGAs that have been used for this purpose, interrelate using a great number of interconnections. In general, this emulator will be used for evaluating any company's future embedded system application, incorporating the ARM CPU and the AMBA bus.

Concluding, it must be pointed out that the design approach that has been used in the development of the 802.11 communication processor and has been based on the emulator board, has helped us to pinpoint many rare conditions which could lead the system in unstable state. This has been proved safer than simulating and integrating the various modules of the chip with the aid of CAD tools, since in a wireless LAN environment, it should be considered that many similar elements, distributed in the network area, coexist and contend the same transmission medium.

The final result of that project will be productized and will be distributed in a rapidly growing market worldwide. In addition, the ARM based MAC chip will become a standard off-the-shelf product (distributed by Atmel/ES2) that can be used by others planning product development for the WLAN market.

References

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[‡] The V-Net project is executed in the framework of the Open Microprocessor Initiative (OMI), and its aim is to implement the V-Net adapter card for demonstrating the use of OMI developed tools and design practice to rapidly develop system configurations that include integration of embedded CPU cores with application microcode.