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The IEEE International Symposium on Industrial Electronics

ATHENS, JULY 1995

A VARIABLE FREQUENCY CONTROLLER FOR THREE PHASE DC/AC INVERTERS

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Abstract — In this paper a multiprocessing system for variable amplitude/frequency control of three phase DC/AC power inverters is presented. The controller consists of four microcontrollers connected in a master-slave configuration. A single microcontroller is used for generating the PWM pulses of each phase and a master microcontroller for determining the system operational parameters. Each phase microcontroller operates as a state machine with analog feedback capabilities and uses an internal look-up table for specifying the duration of the open-loop PWM pulses. Variable frequency is achieved by controlling the clock of the phase microcontrollers, while the modulation depth is determined by the master controller, using an unidirectional high speed synchronous link. The modulator can be used for generating sinewaves in a large frequency range (from 6.25 Hz up to 100 Hz), has very good resolution (0.2% up to 0.4%) and is transient free in amplitude/frequency changes.

Keywords: *PWM modulator, DC/AC power inverter, microcontroller.*

I. INTRODUCTION

Pulse Width Modulation (PWM) techniques have been extensively used to build inverters which generate regulated AC output from DC voltage sources [1]. The main application of this type of inverters is for variable speed induction motor drives, while they are also suitable to be fed by the variable dc output of a photovoltaic array [2]. Various implementation techniques have been proposed using either analog or digital methods, having different characteristics in relation to the depth of modulation, frequency regulation, harmonics elimination, stability etc. Analog based techniques have high accuracy and wide range of frequencies, but require high precision components and synchronization problems are encountered when high switching frequencies are employed [3]. The microprocessor based controllers can be easily manipulated and are free from drift and disturbances but the on-line computation for generating the PWM signals is considered laborious and time consuming [4], whereas the Eprom-based controllers exhibit large memory requirements and a high cost of development and implementation [5].

The proposed multiprocessor PWM controller can be used for generating variable amplitude/frequency sinewaves, with low cost and high stability. The controller operates in a large frequency range (from 6.25 Hz up to 100Hz), is transient free in frequency/amplitude changes, has a very good resolution, and due to the used technology, is compact and highly reliable even in a very noisy environment. The proposed hardware platform can be used to implement various PWM techniques, but in the following discussion the High Switching Frequency Sinusoidal PWM method is used [6]. The HSF-SPWM method uses fixed position of the starting edge of each PWM pulse, instead of fixed position of the PWM center used in symmetric regular sampled PWM methods. In its analog based implementation, the HSF-SPWM technique compares a reference signal, a sinewave of desired frequency, to a modulating triangular wave of much higher frequency and a PWM pulse train is generated. In the microcontroller based implementation, the crossing points of the sinewave with the triangular wave are stored in a look-up table and the PWM pulse train is generated by scanning this table using a state machine. In this paper, the implementation of the HSF-SPWM technique for variable output conditions using multiple microcontrollers is described.

In Section II, the architecture of the proposed modulator is given, emphasizing the functionality of each processing module, while in Section III, experimental results of the modulator performance are presented.

IEEE Catalog Number: 95TH8081

II. The Modulator Architecture

A block diagram of the multiprocessor modulator is shown in Fig. 1. The modulator uses four fast microcontroller units in a master-slave configuration, and a digitally controlled VCO. The master MCU (MC68HC11F1 MCU of Motorola Inc.) determines and manages the inverter parameters and controls the operational conditions of the three slave MCUs. Each slave MCU (MC68HC711E9 MCU of Motorola Inc.) implements a PWM state machine with analog feedback capabilities. It contains a look-up table with the duration of the PWM pulses and generates the two complementary PWM pulse trains with no pulse overlapping. The three slave MCUs contain the same firmware and are synchronized by the master MCU for generating the three phase control signals. The slave MCUs firmware is independent from the required output amplitude/frequency characteristics and forms a state machine which uses the internal look-up table for determining the number of their processing stages and the parameters of each stage.

Figure 2 shows the PWM state machine functional modules. Each MCU includes RAM, EPROM, A/D channels and programmable timers, which allow the development of a state machine with both analog and digital functionality. The MCUs are driven by a clock of variable frequency, which is determined by the master MCU using the digitally controlled VCO. This can be done due to the fully static design of the MCU chips [7]. Figure 3 explains the state-machine processing diagram. An A/D channel is used to sense the line conditions and, based on the total system lag, the duration of each PWM pulse is determined using the current (open loop) look-up table value, the value of the A/D conversion and the value of the pulse duration used k-steps previously. The k-steps delay is equal to the total system lag. This method allows the use of the controller in various inverters with different output filter characteristics and the proper selection of the k-value minimizes the output sinewave distortion. Each PWM state machine generates also a 'polarity discrimination' signal which drives the power push-pull configuration for generating the output sinewave, since each PWM pulse train is unipolar and has a period equal to the half of the period of the output sinewave. The state machine uses also a modulation depth parameter for amplitude control and the scanning step parameter, which

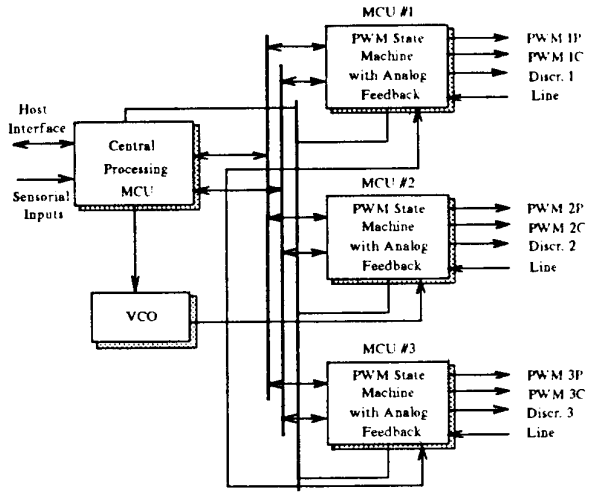


Fig. 1. The modulator block diagram.

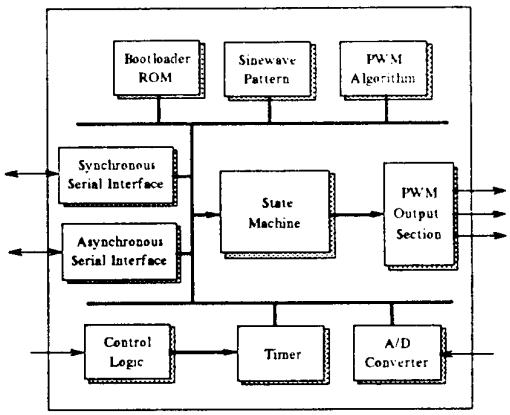


Fig. 2. The PWM state machine diagram.

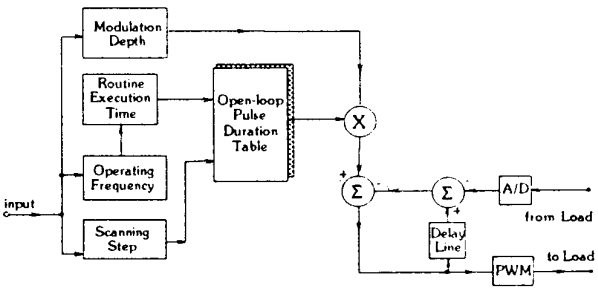


Fig. 3. The firmware processing states.

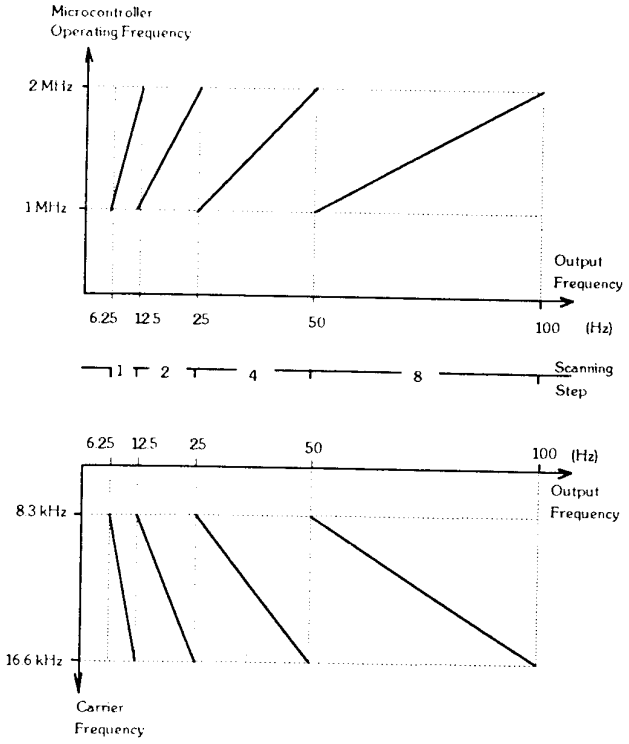


Fig. 4 System operational conditions.

along with the MCUs operating frequency, determine the harmonic content of the generated sinewave.

The master MCU regulates the frequency and the amplitude of the inverter either by using up to seven analog inputs (e.g. from sensors used in photovoltaic systems) or by receiving control commands via an on-chip serial communication interface. The master MCU acquires the 'polarity discrimination' signal and the line conditions of each phase, measures the frequency and amplitude of the inverter output sinewave and makes the appropriate adjustments to phase controllers parameters for achieving the required modulator performance. It can also report the results to a locally or remote based terminal, using its asynchronous communication link.

Each PWM state machine contains 1328 values of pulse duration for each sinewave cycle, which result to a switching frequency between 8.3 KHz and 16.6 KHz depending on the output frequency. The output frequency range (from 6.25 Hz up to 100Hz) is divided to four regions, each one having its highest frequency equal to the double of its lowest frequency (Figure 4). Each region is associated with a scanning step value used by each slave MCU for scanning the PWM look-up table. This is due to the used VCO, which has a linear area of one octave, resulting to VCO output frequency between 4 MHz and 8 MHz and MCUs clock between 1 MHz and 2 MHz, since an on-chip prescaler is used. The digitally controlled VCO consists of the MC1408 D/A converter, the MC1648 VCO and the MC10H350 level translator. The D/A converter is connected to the master MCU bus using a 74LS374 octal D-FFs IC and drives the VCO circuit. The VCO uses the MV1401 varactor in its parallel tank circuit for achieving frequency stability and linearity, while the MC10H350 MECL-to-TTL level translator is used for driving the slave MCUs clock.

When the modulator output frequency has to be changed, the master MCU determines the VCO frequency and the scanning step parameter using the function shown in Figure 4. The selection of the frequency region is done by using the values of two bits, controlled by the master MCU which determine the scanning step of the prestored look-up tables. For frequencies from 6.25Hz up to 12.5Hz, the step is equal to 1 while for the 50-100Hz region the scanning step becomes 8.

The master MCU controls the depth of modulation, which is directly related to the output voltage regulation, by using an on-chip unidirectional high speed (1Mbit/sec) synchronous link, the so called synchronous peripheral interface, SPI. The PWM state machines have been configured in a non-interrupting mode. Each time a new modulation depth is defined, the master MCU stores the new modulation value in the SPI data register of each slave MCU and this value is used when the next value of the look-up table is scanned.

During the modulator start-up, the master MCU drives the reset signal of each slave MCU with a 120^{o} time difference, so the generated sinewaves have also a 120^{o} phase difference. In order to simplify the start-up procedure, the modulator initial output condition has been set to 50 Hz and at the end of the first cycle the modulator output takes the value determined by the sensorial inputs. Figure 5 shows the modulator start-up procedure with 60 Hz, as the initial output conditions.

From the above description it can be easily concluded that the amplitude resolution is 0.4% while the frequency resolution varies from 0.2% up to 0.4% depending on the inverter output frequency. When the inverter drives inductive loads, the phase controllers detect the regeneration intervals, cease the generation of PWM pulses and generate a constant frequency pulse train to feed back the reactive power generated on the load to a

capacitive component. During a regeneration interval, the deployment of the PWM algorithm continues, although the respective PWM pulses are not generated.

III. Modulator Experimental Results

Figures 6a and 7a show the inverter single phase output for upward and downward signal conversion. The experimental conditions are: lower frequency 40Hz/modulation depth 0.4 and higher frequency 60Hz/modulation depth 0.6. Figures 6b and 7b show the harmonic content of these signals as the parameters change. For generating these power distribution figures, the initial signals were sampled at 5 kHz, using the DT2814 data acquisition board of Data Translation Inc. Then, they have been processed using the MATLAB FFT function (128 samples FFT), by splitting the original signals in 64 overlapped regions. Each region lasts for 25 msec.

The sinewave fundamental frequency, F_{out}, is given by the following equation:

$$F_{out} = st.F_c/2.N.p_r.m_c \quad (1)$$

while the first harmonic is in the area of:

$$2.N.F_{out}/st \quad (2)$$

where

F : VCO maximum output frequency,
F_c : VCO output frequency ($F/2 < F_c \leq F$),
p_r : MCU prescaler value,
N : number of stored samples (half-sinewave),
st : look-up table scanning step, and
m_c : number of CPU cycles per executable loop.

In the implemented modulator, the following values have been used:

F : 8 MHz,
p_r : 4,
N : 664, and
m_c : 120.

The modulator frequency stability depends only on the VCO stability, while its response to new output conditions depends on VCO response time and on SPI transfer rate. In all cases the modulator response is a few μsecs, as it has been shown in the experimental results.

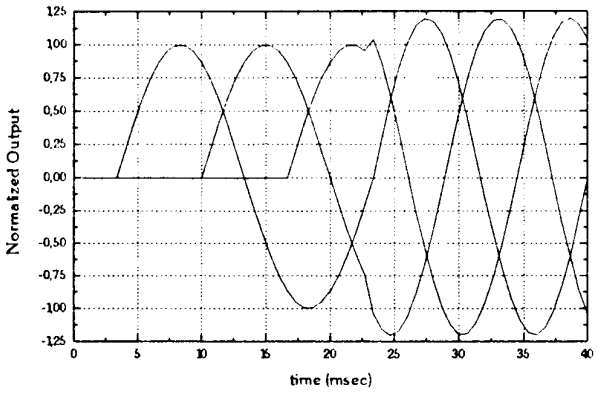
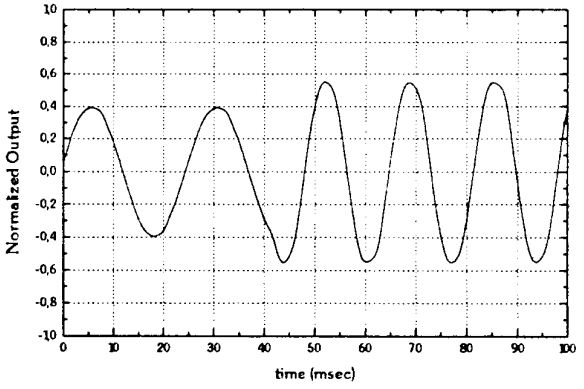
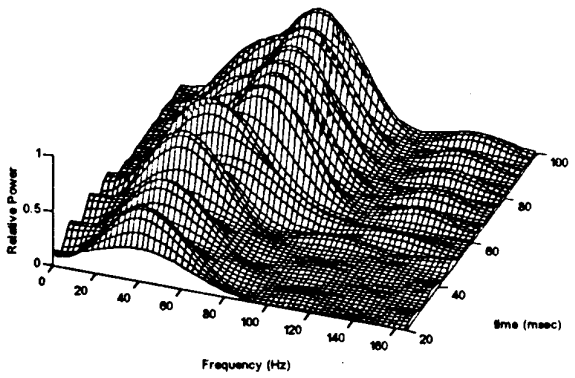


Fig. 5 Modulator start-up procedure.



(a)



(b)

Fig. 6. Output change from 40 Hz/0.4 to 60 Hz/0.6
(a) Single phase output.
(b) Power distribution versus frequency and time.

IV. Conclusions

A multiprocessor-based modulator used for variable frequency three phase DC/AC power inverters has been described. The modulator achieves variable frequency by modifying the circuit operational speed, while keeping its processing procedure constant. Its main advantages are its ability to operate in a large frequency range, and the very good resolution it provides in determining its output frequency and amplitude.

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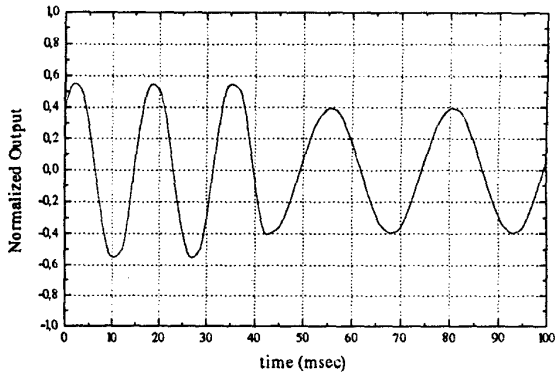
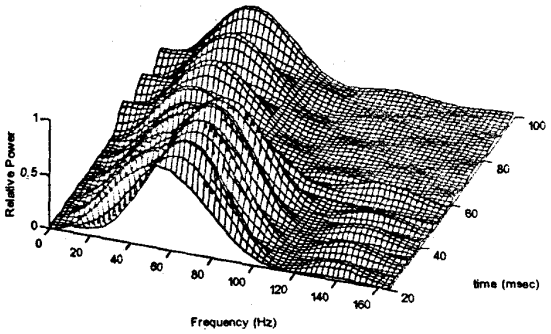


(a)



(b)

Fig. 7. Output change from 60 Hz/0.6 to 40 Hz/0.4
(a) Single phase output.
(b) Power distribution versus frequency and time.