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A Real-time Test-bed for Prototyping Cell-based Communication Networks

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A Real-time Test-bed for Prototyping Cell-based Communication Networks

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Abstract: **This paper presents the basic components and configurations of a real-time test-bed developed for prototyping cell-based communication systems. Although it was initially developed for demonstrating the effectiveness of compression and adaptation techniques in 3DTV transmission over B-ISDN, the test-bed can also be used for measuring the performance of various services and applications over B-ISDN and other cell-based networks. The hardware has been based mainly on FPGAs, allowing the implementation of various communication functions following either the CCITT recommendations or proprietary access protocols.**

I. INTRODUCTION

In recent years one of the major efforts in communication systems development was to determine a flexible and service-independent access technique for use in local and wide-area networks. This method was called Asynchronous Transfer Mode (ATM) and is based on switching or relaying fixed length cells [1], [2]. The Broadband-ISDN and the Synchronous Optical Network (SONET) technologies were the areas of initial application of ATM, but soon the people working on LANs development considered the introduction of this technique in the LAN environment [3]. This is due to its efficiency in network bandwidth and cost-effectiveness of handling all types of services.

Since the ATM functionality forms a low-level bearer service independent of the supported applications, adaptation functions must be performed for enhancing this low-level service to distinct classes of applications. Four different service classes have been defined so far and five different types of adaptation functions have been proposed.

The work presented in this paper originated from the need to demonstrate the performance of an application over B-ISDN under various traffic conditions, controllable by the user and was expanded for covering a number of issues related to the introduction of the ATM technology in the LAN and the Customer Premises Network (CPN) environment. The Laboratory of Electromagnetics participates in the RACE II project "Digital Stereoscopic Imaging and Applications-DISTIMA" [4] for developing the User-Network Interface (UNI) hardware for testing the transmission of 3DTV over existing B-ISDN installations and for developing a real-time network emulator for measuring and demonstrating the performance of the project-developed equipment under various traffic conditions (mean delay, delay jitter and bit error rate). The developed hardware satisfies the CCITT recommendations but, due to its architecture, is very versatile to support a number of different configuration.

In Section II a concise description of the various network topologies and communication technologies that will be covered by this test-bed will be given, while the detailed presentation of the test based architecture will be given in Section III. Section IV emphasizes on the FPGA-based implementation of communication components. Finally, two case studies are presented in Section IV, first the configuration of the DISTIMA demonstrator and second, the FDDI-ATM LAN interworking demonstrator.

II. ATM IN COMMUNICATION SYSTEMS

The ATM was based on virtual channel connections established before actual data transfer and , this connection-oriented characteristic leads to the connection of a single terminal at a given access point of the ATM network. Actually, multiple terminals share a given access point and different services are integrated in the UNI. The concentration of terminals through a single UNI form a CPN. The CPN forms a special type of network at the customer side and there are different types of CPN with different service requirements like bit rate, error performance, throughput and different structural requirements like flexibility, expandability, interworking etc. Since CCITT has not determined how the terminals of a CPN must be interconnected, various topologies have been proposed. Fig. 1 shows the topologies of CPNs that will be considered appropriate for implementation by the test-bed components.

In the LAN environment, the ATM is also used as the transferring mechanism but different functionality is achieved since a mixed topology of shared medium and dedicated lines to each node are used. Various medium access techniques have been proposed and a number of requirements must be fulfilled by the ATM LANs in order to pass easily from current ATM technology to the new ATM LANs era.

The physical connections of CPN nodes are point-to-point channels between adjacent nodes or between network switches, interfaces and hosts. These channels can use various transmission media, like coaxial cable, fiber etc and support various transmission speeds and formats (like pure-

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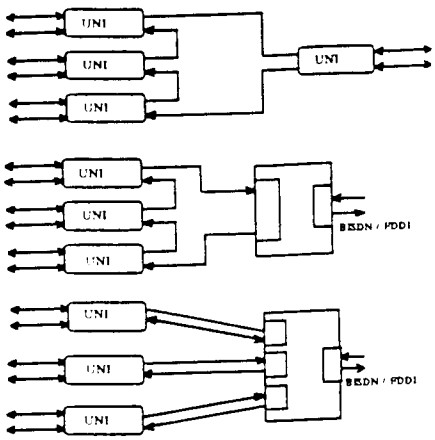

Fig. 1. CPN and LAN Configurations.

ATM and framed-ATM). The network switching functions can be performed either at local switches or using algorithms distributed in the LAN nodes.

Since all the above mentioned options are still under consideration while the basic ATM modules have already been clarified by international organizations, an analysis was carried out in order to determine a flexible and easily adaptable hardware configuration, capable to be used for building a lot of experimental networks with the minimum of modifications. The capability to support a number of different types of terminals through an UNI was a necessity for minimizing the total cost. On the other hand, the need to use testing tools for generating traffic conditions which are met in large installations, was obvious and the need of an expandable system for network conditions emulation was determined.

Considering these requirements, a common system architecture for the network nodes and the testing tools was decided and only two types of boards were developed for all the previously described functions. The system architecture is based on a multiple high-speed bus subsystem which interconnects a central unit with multiple peripheral units. The network emulator has a modular structure since it uses the same types of boards for implementing the traffic conditions of different virtual channels under the control of a central computer. The first board type, which is called User Network Interface (UNI), implements the physical and ATM layer functions and can support various transmission media types. The second board type, which is called emulator board (EB) is a reconfigurable board and implements either the delay and error functions of a single virtual channel, or acts as the node management unit or provides a low-speed interface to external equipment using the GPIB interface.

III. The Real-Time Test-bed Architecture

Although the developed hardware can support the various topologies discussed in the previous section, the basic configuration of the real-time test-bed is the one shown in Fig. 2. In this configuration, two nodes are used and a network emulator. Each node implements the UNI interface and supports up to eight terminals or services like computer data, video and voice, multimedia applications, network interconnections devices etc. The service adaptation functions to the ATM must be provided by the service user. Each node has been implemented in a VME chassis and the boards are double height Eurocards. The network emulator uses two UNI interfaces with multiple emulator boards for each UNI in order to support traffic conditioning on multiple virtual channels in each direction. The emulator boards are controlled by a host computer via the GPIB interface. The network emulator has two backplanes, one for each UNI and the operations of the two directions are completely independent, although they can be synchronized by the emulator host.

The interconnection of the UNI board with the various service (or terminal) adapters, node management unit or emulator boards is performed via the node internal bus. As it is shown in Fig. 3, two independent data paths, one for cell transmission and the other for cell reception are used and the transfer rate in each bus is 20 Mbyte/sec. There is also a Control Bus which is used by the management unit or from a local CPU to control the functionality of the various Terminal Adapters (TA). The TxBus and the RxBus have similar functionality and use 16-bit wide data buses. Due to the constant length data transfers, there is no typical address bus in these sub-buses but they use a 'board selection' utility in relation with a number of read/write cycles for transfering a cell payload. The TAs use some indication lines for reporting to the ATM controller of the UNI their availability for data transfer. During each data transfer cycle, the clock generated by the ATM board is used to coordinate the data transfer and no interlocked handshaking signals are used.

The UNI board is composed of three submodules which implement the ATM layer and the two sublayers of the physical layer, the Physical Medium Dependent (PMD) and the Transmission Convergence (TC). Fig. 3 shows the UNI board architecture. The PMD has been implemented on an add-on card so different transmission media, coding schemes and synchronisation methods can be implemented requiring no modifications of the basic equipment. Currently the STM-1 standard electrical interface has been implemented at 155.52 Mbit/sec. The CMI coder/decoder has been implemented using ECLinPS ICs. As an 155 Mbit/s Synchronizer, the SYN155 device of TRANSWITCH has been used, which detects frames by performing the frame synchronisation algorithm of CCITT [5]. Although this device was developed for NRZ transmissions over fiber, it has been interfaced to a CMI coder for supporting also coaxial cable transmissions.

The interface with the PMD sublayer is performed by an STM-1 Overhead Terminator device (SOT-3 of TRANSWITCH) which performs section, line and path overhead processing of the STM-1 signal. This STM-1 Frame Controller performs pointer generation with respect to external clock timing in both the transmit and receive directions. The STM-1 Frame Controller multiplexes a pure

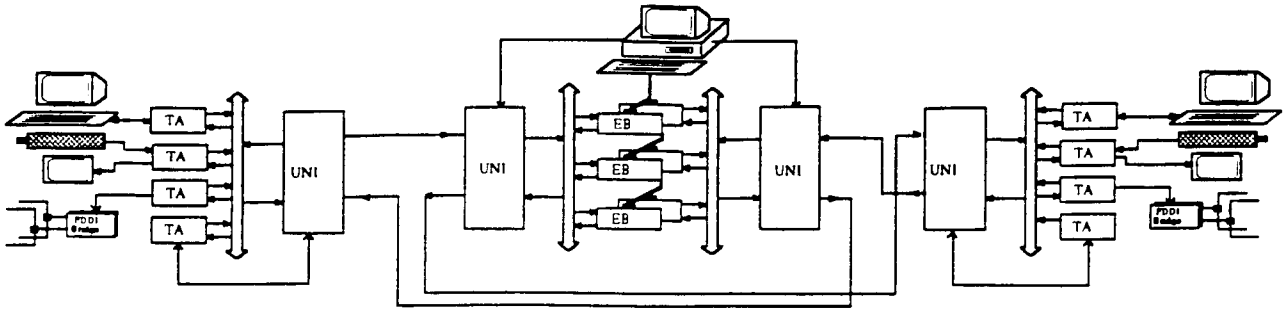

Fig. 2. The real-time test-bed architecure.

ATM cell stream into frames and extracts cells from incoming frames. The TC sublayer uses two FPGAs for implementing the physical layer functions described in [5]. The Tx PHYS FPGA implements the cell delineation function to enable the receiving side of the next UNI interface to recover cell boundaries and generates the Header Error Correction Byte (HEC) of the ATM cell header.The functions implemented in this FPGA also include scrambling of the cell payload and cell rate decoupling by inserting idle cells. The Tx PHYS FPGA receives the first four bytes of a cell header and its 48-bytes payload and inserts complete cells in the output frame. The Rx PHYS FPGA implements the receive direction functions of the TC sublayer. It calculates and confirms the HEC value of the received cells and re-establishes cell boundaries. Cell headers are checked for errors and single-bit error correction is performed whenever it is possible, otherwise the cell is discarded. Received idle cells are suppressed and cell payload descrambling is performed.

The ATM layer has been implemented using an ATM

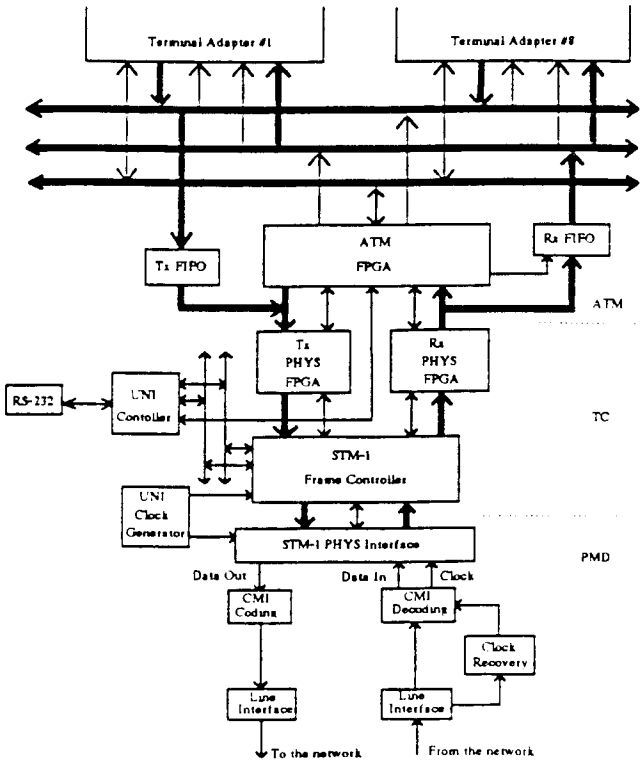

Fig. 3 The User-Network Interface.

Controller (FPGA based) and two FIFOs, one for each direction. The ATM Controller manages the node's internal bus in both directions and multiplexes cells from different service access points and its functionality is completely independent of the Physical Layer functionality. The ATM Controller has been designed to implement the cell assembly/disassembly following the B-ISDN ATM Layer functionality or to support the specific requirements of a medium access protocol. The STM-1 Frame Controller, the TC FPGAs and the ATM FPGA are controlled by a local CPU (UNI Controller) which determines the board functionality. An RS-232C interface gives access to the UNI structure and allows the collection of statistics for further processing.

The Emulator board, which is shown in Fig. 4, is a multi-functional board for implementing network traffic conditions, low-speed terminal adapters and node management functions. The board uses a local CPU which controls the two FIFOs for cell payload reception and transmission. The board has a number of FPGAs for implementing the interface to the internal bus, the cell delay functions and error rate control. The FPGAs architecture is controlled by the local CPU and can be reprogrammed during system operation for implementing various delay functions, mean delay values and delay jitter bounds. The Cell Delay Generator implements the cell delay function and generates the timing of the output cell stream based on the input cell stream interarrival timer, provided by the AAL-ATM Interface Controller and on the locally generated delay values. The Error Rate Control FPGA uses the desired BER of the emulated virtual channel for estimating the cell rejection rate and inserting errors in the cell payload by estimating the single bit error rate probability. The errors are inserted in the cell payload when it is transmitted from the Rx FIFO to the Tx FIFO using a XOR plane, controllable by the Error Rate Control FPGA.

When the emulator board is used as the node management unit, the local CPU is connected with the UNI CPU through the RS232C interface in order to control the ATM Controller's parameters.

IV. Communication Components using FPGAs.

As it was explained previously, two kinds of boards were developed for the test-bed, the UNI-board for implementing the network interfaces and the EB-board

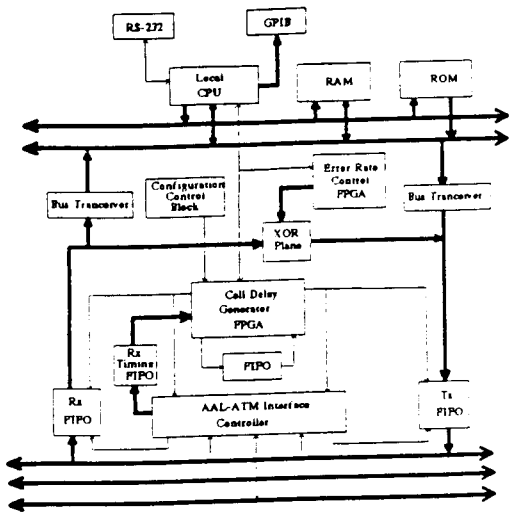

Fig. 4. The Emulator Board.

foremulating traffic conditions, implementing system management functions and providing a simple interface for low-speed applications. In this section the implementation of the Physical and ATM Layer components using FPGAs will be addressed.

The ATM Controller.

The ATM layer provides the multiplexing/demultiplexing of the cells of various connections into the network cell stream. The cell headers are constructed using the information provided by the local CPU or the node management unit. The ATM layer contains two 16-bit wide FIFOs for temporary cell payload storage during cell header processing in the ATM Controller. The controller architecure is shown in Fig. 5. The controller's central unit is the Decision Unit, which determines how the various TAs are served. When there is available space in the Tx FIFO, the Scanning Selector determines which is the next TA that has to be served by using the information provided by the ATM Arbiter. The ATM Arbiter receives a signal from each TA indicating the availability of a cell. The decision is made during the payload transmission of the previous cell and no time elapses between the FIFO availability and the new cell reception. The Tx DMA, a fixed length DMA with no address bus signals, generates the required signals to synchronize the TAs with the ATM Tx FIFO. Whenever the DMA cycle is completed, the cell is ready for transmission to the Physical layer. During the DMA transmission, the Tx Control Unit sets the header's position in the Position Selectable Memory (PSM). The PSM memory is a special purpose RAM with the following functionality: the length of the memory is 32 bytes, organized in 8 block of 4-bytes. Each block contains the first four bytes of a cell header. For each TA, its position in the internal bus is the same with the position of its header in the PSM. The content of each block is updated by the NMU via the SPI when a new connection is established. The PSM output address is determined by combining the respective block pointer and the output of a 2-bit counter which increases when a new clock cycle is generated by the Physical layer. Following this information flow structure, a 400 kcell/sec processing speed has been achieved. The circuit operational speed is 20 MHz and it has been implemented in a XC4005 FPGA of XILINX Inc.

In the receive direction, the value of the VCI/VPI field of each cell header is compared in the Content Addressable Memory (CAM). The CAM memory contains the VCI/VPI values of each TA and generates this value each time a match is detected. The Rx DMA is informed about the destination of the current cell and the cell payload is transmitted to the respective terminal adapter. The content of the CAM memory is updated by the local CPU using the SPI interface. Both the PSM and CAM memory modules are used for providing a direct relation between the static TA board position in the Internal Bus with the dynamic allocation of the

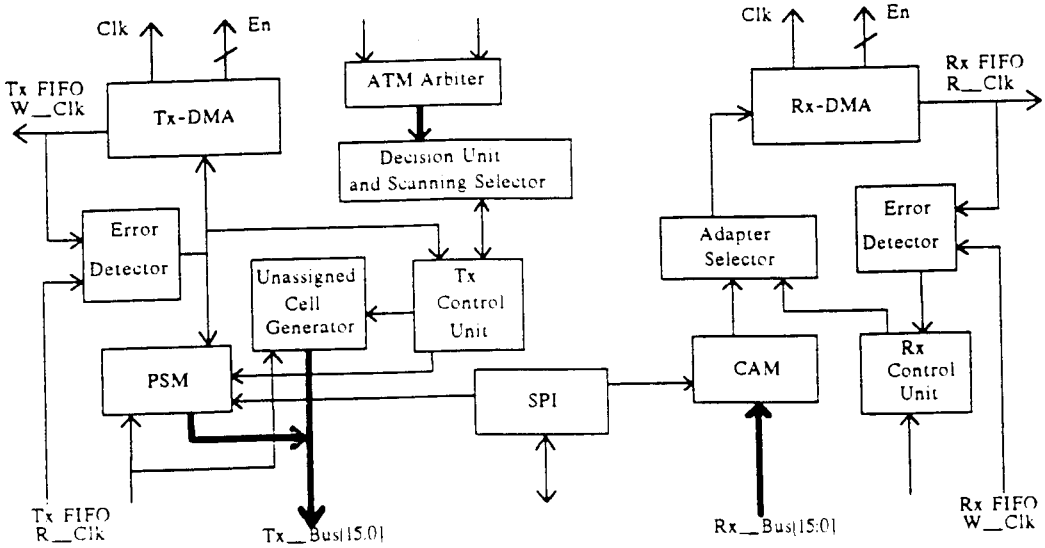

Fig. 5. The ATM Controller block diagram.

VCI/VPI values in the ATM layer. The Error Detector Units supervize the ATM Controller's operation in both directions by validating the integrity of cells' payload stored in the FIFOs, in order to detect and correct errors occured in the write and read cycles of the external FIFOs.

The TC Sublayer Transmitter

The TC transmitter shown in Fig. 6 is used to receive user cells from the ATM layer, to generate the HEC byte of the cells' header and to generate idle cells for cell rate decoupling. The TC interfaces to the ATM via a 16-bit bus for cell payload and header information multiplexing. If no cell is available, the Idle Cell Generator is activated.

When a cell is transmitted, the CRC Generator/Header Buffer is used to generate the HEC field using a HEC byte generation unit implementing the 8-bit CCITT polynomial. The cell payload is scrambled before transmittion to the STM-1 Frame Controller. The whole TC transmitter operation is controlled by the Tx Controller and its operation is synchronized with the network status since the cell stream may be interrupted in any position when the header of a new frame must be inserted in the output stream. The TC transmitter has been implemented in a XC3164 FPGA and achieves a total of 155 Mbit/sec system operation.

The TC Sublayer Receiver

The TC receiver, which is also shown in Fig. 6, performs the receive functions of the physical layer, such as cell delineation, HEC validation and correction, idle cell extraction etc.

The TC Receiver scans the byte stream provided by the STM-1 Frame Controller and perfoms the cell delineation function by means of a parallel HEC byte validation unit. If more than a single error have been detected in the received header, an indication of cell discarding is generated, otherwise the position (byte number and bit position) of the error is calculated and the header correction is performed during the transfer of the header to the ATM layer using a XOR-gate plane. The payload bytes are descrambled when synchonization has been achieved and a internal FIFO is used in the Payload Buffers for delaying the first bytes of a cell's payload until the results of the header processing are available. Whenever an idle cell is detected, the payload buffers are cleared and the cell is discarded. The TC receiver has been implemented in a XC3195 FPGA.

V. Test-Bed Case Studies.

The presented test-bed will be used in two different case studies. The first case is the DISTIMA demonstrator where the test-bed will form its transmission part. The scope of the transmission part of the DISTIMA demonstrator is to provide the required communication subsystem for 3DTV information exchange between the encoder of a transmitting node to the decoder of a receiving node, following the ATM technology. The total path contains the camera, the video encoder, the adaptation functions at the coder side, the ATM transmitter, the transmission medium (at least an emulated ATM switch must be included), the ATM receiver, the adaptation functions at the decoder side, the video decoder and the display. The possible capabilities of the transmission subsystem were determined to be the following:

- provision of transmission frame adaptation and cell handling procedures, and
- provision of the required bit timing and physical dependent functions of the transmissison channel.

Fig. 7 shows a block diagram of the demonstrator's architecture. The 3DTV camera generates five different information sources which are multiplexed in a single CBR bit stream of 10 Mb/s after compression using the MPEG 2 algorithm. Then the bit stream is adapted to the ATM services by using the AAL-type 1, for mapping the higher

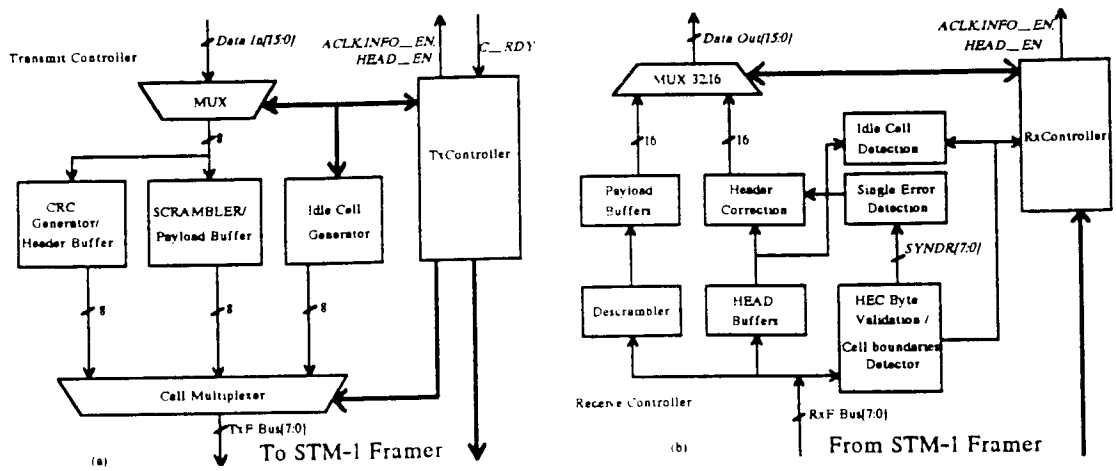

Fig. 6. The TC Sublayer components block diagram: (a) the transmitter, (b) the receiver.

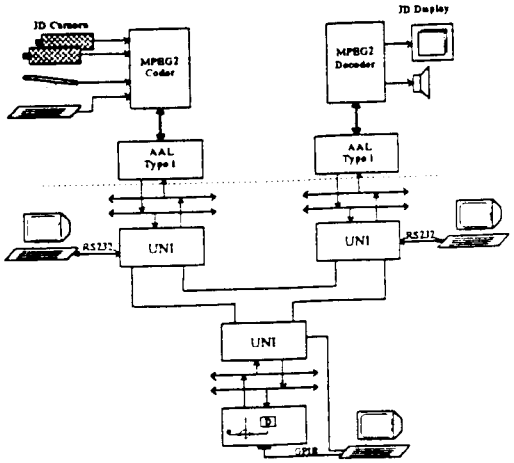

Fig. 7. The DISTIMA demonstrator.

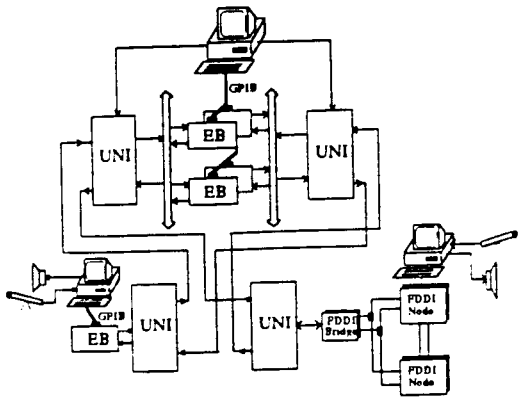

Fig. 8. The FDDI-ATM demonstrator.

layer protocol data units into the payload of the ATM cells and vice-versa. For this demonstration the manual set-up of the network signalling was selected since the same configuration will be tested in an existing B-ISDN installation in Europe without using the network emulator. Using the network emulator, the performance of the MPEG coder/decoder for CCITT approved test sequences and real-time shooting under specific traffic conditions will be examined, as well as the service enhancement achieved using a specific implementation of AAL type 1. The synchronization achieved using various values of cell delay jitter and cell loss rate are of great importance.

The second case will be an FDDI-ATM LAN demonstrator. As it is shown in Fig. 8 the test-bed will be organized as a single ring ATM LAN with a network emulator consisting of two independent parts. Network emulation will be performed independently for the two directions of a full duplex communication. In this case the configuration will be used to demonstrate the transmission of computer data and compressed voice between two nodes, one attached to a ATM LAN UNI and the other to a FDDI network interconnected to the ATM LAN using a bridge. The FDDI node consist of the PC-based FDDI development boards of Motorola (M68FDDIADS). Using this configuration the TCP/IP suite for file transfer over ATM and FDDI will be examined and an inter-office communication system with constant and variable bit rate vocoders will be demonstrated.

CONCLUSION

In this paper the architecture, implementation issues and case studies of a real-time test-bed for prototyping cell-based communication networks were presented. The test-bed has been developed using two kinds of reconfigurable boards which implement various network architectures based on the ATM technique. The test-bed can effectively emulate various traffic conditions using an expandable architecture, capable to support multiple virtual channel connections. Although the current version of the test-bed satisfies the CCITT recommendations for the STM-1 interface, proprietary protocols and configurations can be implemented and tested as well as various physical medium dependent interfaces. The system's transmission bit rate is 155.52 Mb/s, resulting to a cell processing capability of 366 Kcells/sec and can support a large number of virtual circuit connections of up to 10 Mb/s each.

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