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Multiple Boundary Scan-Paths for Minimizing Circuit-
Board Test-Application Time

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Abstract

This paper presents a technique for minimizing the test-application time of a circuit board designed with boundary scan. The technique is based on the use of multiple boundary scan paths. The paper discusses how the boundary scan paths are selected and provides analytical expressions for comparing test-application times for different boundary scan configurations on a circuit board. The paper shows that for certain circuit board configurations the use of multiple boundary scan paths can result to significant reduction in test application time at the expense of a few additional board I/O.

Key words: Boundary scan; Single test mode; Concurrent test mode; Enhanced single test mode; Multi-chip groups

1. Introduction

Board level testing generally consists of a functional test and an in-circuit test. During the in-circuit test, test vectors are applied to individual chips on the board and the chip-response is captured and evaluated for each chip on the board. With the increased use of surface mount technology and the reduction in package lead spacing, individual chips may no longer be accessible for incircuit testing [1]. One way to overcome this problem is to use boundary scan which gives serial access to the components on the board without the need to probe the individual I/O pins [2]. The serial access is provided through a standard interface, known as IEEE S.1149.1, and is performed from the board edge connector using 4 pins [3]. In this case, the chip-level test vectors that are derived assuming all I/O are accessible in parallel, have to be modified to conform to the serial access. This serialization process could easily result to board-level test sets of millions of vectors which in turn can cause potentially unacceptable increases in test application times. Therefore, approaches are needed for efficient translation of chip test sets to boundary-scan board test sets. Furthermore,

techniques for applying the board-level test sets need to be developed so that test application time is minimized. This paper presents a technique aimed at reducing the test application time of a boundary-scan based board by using, multiple boundary-scan chains. The test application time of interest here is the time expended for internal test [3] where each chip on the board is tested for functional integrity with its individual test set.

2. One boundary-scan path techniques

Three different techniques for test pattern application in a single boundary scan path organization have been reported in the past [4]. These techniques are the Single Test Mode (STM), the Concurrent Test Mode (CTM), and the Enhanced Single Test Mode (ESTM).

In the STM technique every chip in the boundary-scan path is considered and tested individually while the other chips are in the bypass mode of the S.1149.1 protocol. In this case each bypassed chip contributes one clock cycle delay to the boundary scan instead of a delay equal to the number of I/O in that chip. When testing the ith chip in the boundary scan path, each vector in the ith test set has to be shifted for j clock periods, where j is the number of chips in the scan-path physically located prior to the chip that is under test (CUT). In addition, the inputs and outputs of the CUT must be taken into account. Place-holding bits must be positioned at the outputs while shifting a vector in the boundary scan and the inputs must be ignored while shifting out the response. When the vector is applied to chip i, the generated response is shifted out all the way through the serial output port (i.e. TDO) of the boundary scan standard interface, before a new vector is shifted in. The advantage of this technique is its implementation simplicity, which however, is gained at the expense of long test application times.

Concurrent test mode (CTM) refers to the application of test vectors to all chips on the board simultaneously. Unlike the previous case, none of the chips are initially in the bypass mode while testing of the board is initiated. Board-level boundary scan vectors are formed by interleaving the first vector of chip M with the first vector of chip $M - 1$, and so forth. The process of vector interleaving is repeated for the subsequent vectors of every chip until the shortest chip test set is exhausted. Once the test set of a chip in the scan path is exhausted, testing of the board is halted and a new instruction sequence is issued in order to place the chip with the exhausted test set in the bypass mode. In the worst case, the board testing is halted $M - 1$ times before all vectors have been applied. The advantage of CTM is the concurrent application of test vectors to all chips on a board. However, the drawback of this technique is the extra shifting that is necessary to scan test vectors through the bypassed chips.

The enhanced single test mode (ESTM) technique was proposed as a means of reducing the extra test vector shifting in CTM. In ESTM the bypassed chips preceding the CUT are treated as a pipeline where portions of subsequent test vectors are stored in the bypass register of every chip preceding the CUT. The test response could also be temporarily stored in the bypass registers of the chips physically located after the CUT in the boundary scan path. These bypass registers, whose contents are not affected by the application of the next test vector, act as a pipeline register storing the test responses before they are shifted out.

The implementation of the ESTM complies with the IEEE S.1149.1 standard specification only if different TMS signals are used for chips operating at different modes (i.e. Bypass, Internal Scan). For many applications this requirement may represent an unacceptable I/O and routing overhead for the board design. In this case ESTM can be

implemented by including a single bit data register in the S.1149.1 design which is selected with an optional scan instruction. This register operates similarly to the bypass register, the only difference being that it maintains its data (instead of reset) during the update-DR cycle [3].

For the rest of this paper the following terminology will be used:

M: the number of chips on a board.

l_j: the length of the test vector set for chip j.

p_j: the total number of pins of chip j included in the scan path. p_j consists of ij input pins and oj output pins.

S: the required time to scan an instruction into the instruction register of all chips on the board.

A_j: the application time of a test vector for chip j. This time includes the data register update time and the application circuit delay.

The required test application times for the STM and the ESTM techniques are [4]:

$$T_{STM} = M \cdot S + 2 \sum_{j=1}^{M} p_j l_j + \sum_{j=1}^{M} A_j l_j + (M - 1) \sum_{j=1}^{M} l_j$$

(1)

$$T_{ESTM} = M \cdot S + \sum_{j=1}^{M} l_j \cdot \max(ij, oj) + \sum_{j=1}^{M} A_j l_j. \quad (2)$$

3. The multiple boundary scan paths technique

The single boundary scan path techniques do not take into account that a board with M chips may contain several chips that are identical in terms of function and I/O configuration. In this case proper organization of the boundary scan in multiple paths may allow the parallel application of test vectors to all the chips of the same type, and there-

fore the reduction of the board test application time.

The choice of multiple boundary scan paths on a board is using the notion of a group. A group is defined as a collection of chips of the same type. Single-chip groups are groups containing a single chip, while multiple-chip groups are groups containing two or more chips of the same type. The notation related to the notion of a group is given below and it will be used throughout this paper.

η_m: the number of multi-chip groups

η_s: the number of single-chip groups

N_i: the number of chips in group i

L_i: the length of the vector test set for a chip in group i

P_i: the number of pins in the scan path of a chip in group i (I_i Input Pins + O_i Output Pins)

A_i: the application time of a test vector to a chip in group i

S_1: the required time to scan an instruction into the instruction register of all the chips in the scan path.

The organization of the Multiple Boundary-Scan Paths is shown in Fig. 1. There are N_1 Boundary Scan Paths, where N_1 is the greatest number of chips in a group. The first scan-path consists of all the single-chip groups and one chip from every multi-chip group.

The single-chip groups are connected next to the input of the path and the chips from the multiple-chip groups are connected in the following order: If $N_K > N_l$, then the chip from group K is nearer to the output than the chip from group l. If $N_k = N_l$, the order of connection between the K-group chip and the l-group chip is not significant. However, the same order must be kept in the organization of all the paths. The rest of the chips form a new group set $\{N_{\eta m} - 1, N_{\eta m - 1} - 1, ..., N_2 - 1, N_1 - 1\}$ which provides the chips for forming the rest of the scan-paths using the above procedure. During testing, vectors are applied first to the single-chip groups. Scan
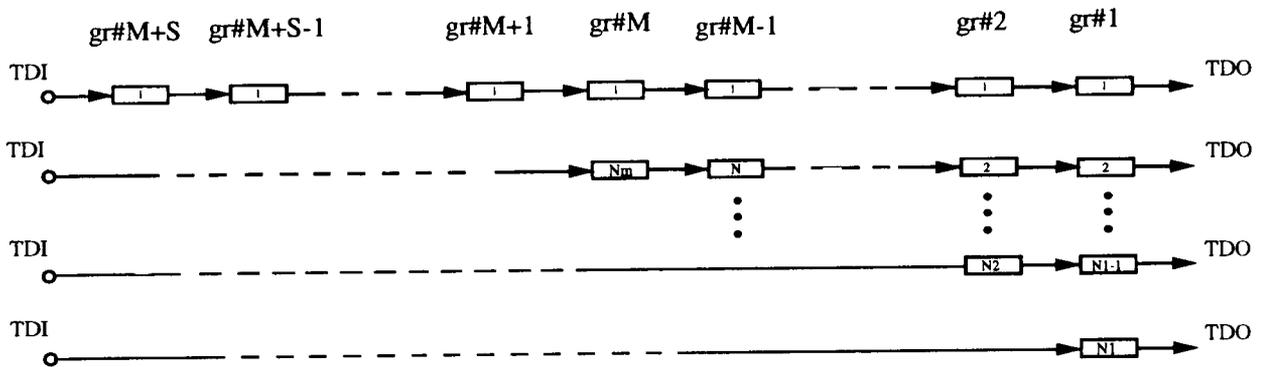
Fig. 1. The multiple boundary-scan path organization.

paths that do not contain single-chip groups are idle at this time.

When the testing of a single-chip groups is finished, the testing of the m-multi-chip group begins by exercising all the required boundary scan paths. All the chips in their paths are in bypass mode except the chips of the m-multi-chip group. The ESTM technique for every path is used and the same procedure is repeated until the testing of the scan chain for all the multi-hip groups is completed. The advantages of this technique are:

(i) The vector set of a multi-chip group is applied only once instead of N_i times, where N_i is the number of chips of this group, and

(ii) Availability of test response from identical chips can potentially be used for test evaluation in real time.

The trade-off for these benefits is the addition of board I/O. The required time to apply a test vector set to a chip, independently of the type of group it belongs to, is:

$$T_i = S_1 + (\eta_s + \eta_m - i) + I_i + (L_i - 1)$$

$$\cdot \max(I_i, O_i) + L_i A_i + (O_i + 1)$$

and the total time (T_{MBSP}) is

$$T_{MBSP} = \sum_{i=1}^{\eta_m + \eta_s} T_i = (\eta_m + \eta_s) \cdot S_1 + \sum_{i=1}^{\eta_m + \eta_s} I_i$$

$$+ \sum_{i=1}^{\eta_m + \eta_s} (L_i - 1) \cdot \max(I_i, O_i)$$

$$+ \sum_{i=1}^{\eta_m + \eta_s} A_i L_i + \sum_{i=1}^{\eta_m + \eta_s} (O_i + 1)$$

$$+ \frac{(\eta_m + \eta_s)(\eta_m + \eta_s - 1)}{2} \tag{3}$$

or

$$T_{MBSP} \approx (\eta_m + \eta_s) \cdot S_1$$

$$+ \sum_{i=1}^{\eta_m + \eta_s} L_i \cdot \max(I_i, O_i) + \sum_{i=1}^{\eta_m + \eta_s} A_i L_i.$$

The above simplification is based on the assumption that $L_i \gg P_i$ (in general) and $\max(I_i, O_i) > 1$ which yields:

$$L_i \max(I_i, O_i) \gg P_i \max(I_i, O_i) > P_i$$

therefore,

$$\sum L_i \max(I_i, O_i) \gg \sum P_i = \sum I_i + \sum O_i$$

or

$$\sum L_i \max(I_i, O_i) \simeq \sum I_i + \sum (L_i - 1) \max(I_i, O_i) + \sum O_i .$$

The quantity $((\eta_m + \eta_s)(\eta_m + \eta_s - 1))/2$ will in general be negligible compared with the rest of the terms in the expression for T_{MBSP}.

4. Test application time comparisons

Eqs. (1) and (2) can be rewritten, using the group notation:

$$T_{STM} = \left(\sum_{i=1}^{\eta_m + \eta_s} N_i \right) \cdot S + 2 \cdot \sum_{i=1}^{\eta_m + \eta_s} N_i P_i L_i$$
$$+ \sum_{i=1}^{\eta_m + \eta_s} N_i A_i L_i + \left(\sum_{i=1}^{\eta_m + \eta_s} N_i - 1 \right)$$
$$\times \sum_{i=1}^{\eta_m + \eta_s} N_i L_i . \tag{4}$$

and

$$T_{ESTM} = \left(\sum_{i=1}^{\eta_m + \eta_s} N_i \right) \cdot S + \sum_{i=1}^{\eta_m + \eta_s} N_i L_i$$
$$\cdot \max(I_i, O_i) + \sum_{i=1}^{\eta_m + \eta_s} N_i \cdot A_i L_i . \tag{5}$$

For the purpose of comparing the test application times of the techniques discussed, we simplify the test application time expressions by assuming that:

(i) The differences between A_i's are negligible so A_i may be replaced by A.

(ii) The setup time for a path is analogous to the number of chips in the path, so:

$$\frac{S}{S_1} \approx \frac{\sum_{i=1}^{\eta_m + \eta_s} N_i}{\eta_m + \eta_s} .$$

We next define the following parameters:

(i) $p_{gave} = \dfrac{\sum_{i=1}^{\eta_m + \eta_s} N_i P_i}{\sum_{i=1}^{\eta_m + \eta_s} N_i}$: the mean number of pins per chip.

(ii) $p_{ave} = \dfrac{\sum_{i=1}^{\eta_m + \eta_s} P_i}{\eta_m + \eta_s}$: the mean number of pins per chip-type.

(iii) $a = \dfrac{\sum_{i=1}^{\eta_m + \eta_s} N_i \cdot \max(I_i, O_i)}{\sum_{i=1}^{\eta_m + \eta_s} N_i \cdot P_i}$: the mean number of the pin-type (I,O) at the chip level.

(iv) $d = \dfrac{\sum_{i=1}^{\eta_m + \eta_s} \max(I_i, O_i)}{\sum_{i=1}^{\eta_m + \eta_s} P_i}$: the mean number of the pin-type (I,O) at the group level.

(v) $e = \dfrac{\sum_{i=1}^{\eta_m + \eta_s} N_i L_i}{\sum_{i=1}^{\eta_m + \eta_s} L_i}$: influence factor of the grouping approach to test set application time.

(vi) $\eta_{ave} = \dfrac{\sum_{i=1}^{\eta_m + \eta_s} N_i}{\eta_m + \eta_s}$: the mean number of chips per group.

Assuming that L_i, P_i, N_i have little correlation and using the above definitions, we can write the following expressions:

$$a \cdot p_{gave} = \frac{\sum N_i \max(I_i, O_i)}{\sum N_i}$$

and

$$d p_{ave} = \frac{\sum \max(I_i, O_i)}{\eta_m + \eta_s} .$$

Since

$$\sum N_i \max(I_i, O_i) \approx \frac{\sum N_i \sum \max(I_i, O_i)}{\eta_m + \eta_s}$$

$$a \, p_{\text{gave}} = \frac{(\sum N_i \sum \max(I_i, O_i))}{\eta_m + \eta_s} \bigg/ \sum N_i = \frac{\sum \max(I_i, O_i)}{\eta_m + \eta_s}$$

or

$$a \cdot p_{\text{gave}} \approx d \cdot p_{\text{ave}} .$$

Assuming that N_i and L_i have little correlation we can write:

$$e = \frac{\sum N_i L_i}{\sum L_i} \approx \left(\frac{\sum N_i \sum L_i}{\eta_m + \eta_s} \right) \bigg/ \sum L_i = \frac{\sum N_i}{\eta_m + \eta_s}$$

or

$$e \approx \eta_{\text{ave}}.$$

Since $\displaystyle\sum_{i=1}^{\eta_m + \eta_s} L_i$ can be very large, we may assume that:

$$\frac{\left(\displaystyle\sum_{i=1}^{\eta_m + \eta_s} N_i \right) \cdot S}{\displaystyle\sum_{i=1}^{\eta_m + \eta_s} N_i L_i} \approx \frac{(\eta_m + \eta_s) S_1}{\displaystyle\sum_{i=1}^{\eta_m + \eta_s} N_i L_i} \approx 0$$

then:

$$\frac{T_{\text{ESTM}}}{T_{\text{MBSP}}} \approx \frac{e \cdot A + a \cdot p_{\text{ave}} \cdot \eta_{\text{ave}}}{A + d \cdot p_{\text{ave}}} \approx \eta_{\text{ave}} \qquad (6)$$

and

$$\frac{T_{\text{STM}}}{T_{\text{MBSP}}} \approx \eta_{\text{ave}} \cdot \frac{A + 2 \cdot p_{\text{ave}} + \eta_{\text{ave}} \cdot (\eta_m + \eta_s) - 1}{A + d \cdot p_{\text{ave}}}. \qquad (7)$$

From these two equations we can observe that the MBSP speedup strongly depends on the mean value of the distribution of the number of chips in groups. As the number of chips per group increases, the performance of the MBSP increases. For a more accurate measure of the performance speedup, Eqs. (3), (4) and (5) must be used in order to take into account the correlation between L_i, P_i, and N_i.

In Fig. 2(a), the relation between $T_{\text{STM}}/T_{\text{MBSP}}$ and η_{ave} is shown using the analytic expressions above, while Fig. 2(b) shows the respective relation between $T_{\text{ESTM}}/T_{\text{MESP}}$ and η_{ave}.

5. An application example

The Nodal Control Circuit Switch (NCCS) [5] is a mobile, transportable, tactical automatic switching system which provides automatic circuit switching service and nodal control functions. It is modular and is capable of performing functions and services related to the handling of voice and data messages. Applications of the NCSS are in communications systems for use in newly activated installations, and emergency missions. The NCCS was developed by GTE for the US Army.

The Matrix Interface B (MTX-B) is a single printed circuit board which provides decoder and crosspoint functions to the NCSS. This circuit board is used as an example to demonstrate the use of the multiple boundary scan path approach proposed in this paper.

MTX-B is a digital board containing 39 chips. All the chips on this board are off-the-shelf components of various complexities and of various functional characteristics. Although old versions of this design do not include boundary scan, a projected redesign for the board including boundary scan makes this a good example candidate for establishing potential test application time improvements by using multiple scan chains. Fig. 3 shows an engineering drawing of the board.

Based on the multiplicity of components used, six groups of chips can be identified. Each group contains identical chips and the number of chips per group is shown in Table 1.
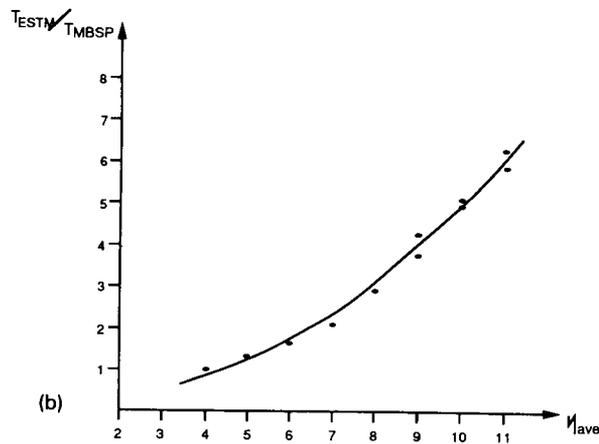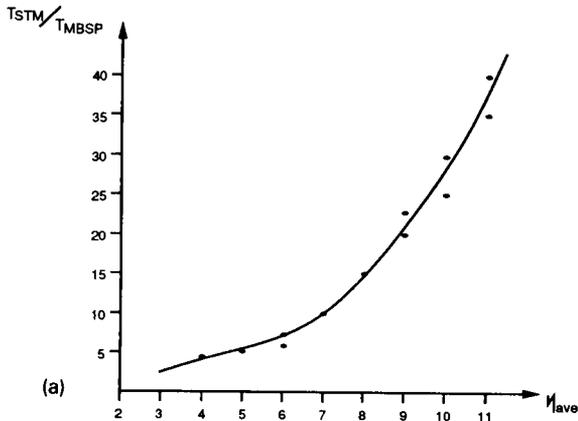
Fig. 2. Test application time speedup versus the average number of chips per group.

The chips belonging to a group are identified with their group number in Fig. 3. In order to demonstrate the test application time speed-up when using multiple boundary scan paths based on the proposed approach, we examined three boundary scan path configurations with different chip groupings. In each case, the speed-up was assessed by using both the analytical

Table 1
Chip groups in the MTX-B Board

Group number	Number of chips
1	9
2	5
3	10
4	3
5	5
6	5

Eqs. (3), (4), and (5) and the estimators given by Eqs. (6) and (7).

The first multiple boundary scan path configuration includes ten boundary scan paths with the chip grouping per path showing in Fig. 4. Using the analytical results in this paper, it is found that $T_{ESTM}/T_{MBSP} = 9.13$ and $T_{STM}/T_{MBSP} = 63.6$ while the estimators yield $T_{ESTM}/T_{MBSP} = 9.25$ and $T_{STM}/T_{MBSP} = 69.49$ respectively.

A different grouping of chips for the same number of boundary scan paths is shown in Fig. 5. In this case, the analytical results are $T_{ESTM}/T_{MBSP} = 7.38$ and $T_{STM}/T_{MBSP} = 51.4$ while the estimated results are $T_{ESTM}/T_{MBSP} = 6.16$ and $T_{STM}/T_{MBSP} = 44.95$. Finally, a configuration with five boundary scan paths and the corresponding chip groupings is shown in Fig. 6. In this case, the results obtained are $T_{ESTM}/T_{MBSP} = 4.55$ and $T_{STM}/T_{MBSP} = 31.68$ while the estimated results are $T_{ESTM}/T_{MBSP} = 4.625$ and $T_{STM}/T_{MBSP} = 34.75$.

The obtained results from this example show that indeed a test application time speed-up is expected when using multiple boundary scan paths. For a given number of scan paths this speed-up strongly depends on the average number of chips per group as was indicated by the analytical results obtained. A good correlation also exists between the analytically computed speed-up and the estimated one. Furthermore, the obtained results indicate that test application times in a boundary scan
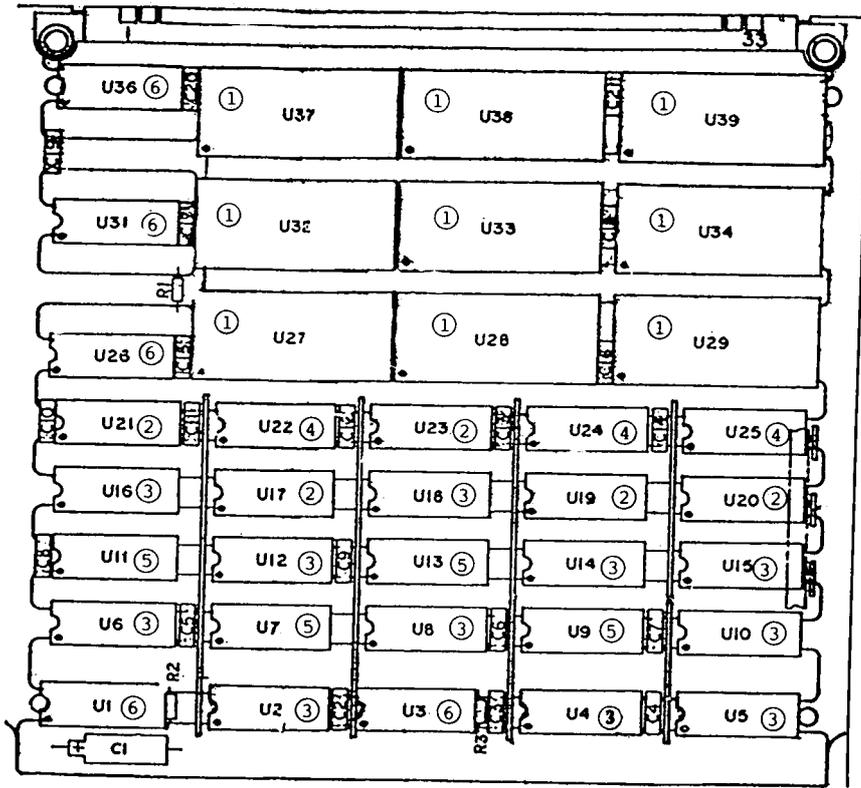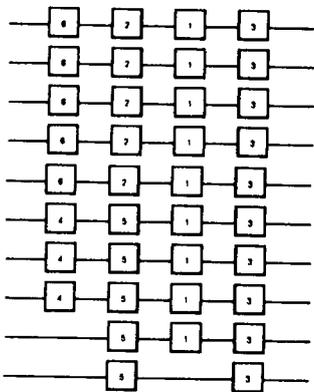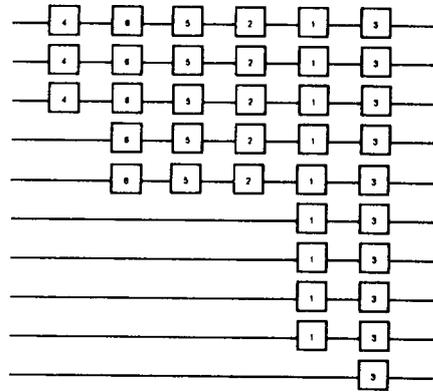
Fig. 3. An engineering drawing of the MTX-B board.

$$\eta_m = 4$$

$$\eta_s = 0$$

$$\eta_{ave} = 9.25$$

Pgave $= 16.9$

Pave $= 17$

Fig. 4. A multiple boundary scan path configuration for the MTX-B with ten paths.

$$\eta_m = 6$$

$$\eta_s = 0$$

$$\eta_{ave} = 6.16$$

Pgave $= 16.9$

Pave $= 17$

Fig. 5. A ten scan path configuration for the MTX-B with different nave.

$$M_m = 8$$

$$M_s = 0$$

$$M_{ave} = 4.626$$

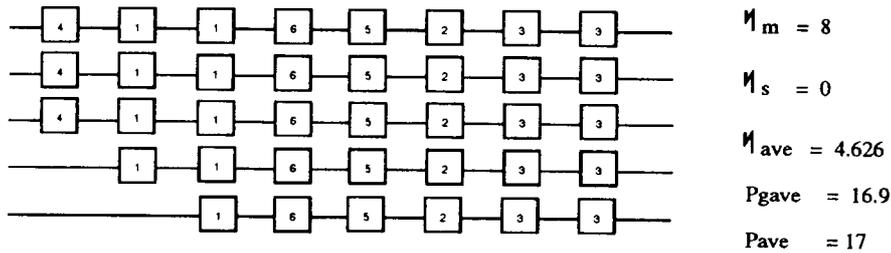$$Pgave = 16.9$$

$$Pave = 17$$

Fig. 6. A five scan path configuration for the MTX-B.

environment (for internal test) can vary widely depending on the way the test is applied. The Enhanced Signal Test Mode outperforms the commonly used Single Test Mode by 7 to 1 in this example. The Multiple Boundary Scan Path approach offers the fastest application times and the time speed-up seems to be almost linear with the number of the scan paths used. Although grouping of chips in the scan paths used in this example did not follow a particular algorithm, the results obtained indicate that groupings should be formed so that the average number of chips per group is maximized (η_{ave}).

6. Conclusions

This paper presented an approach for reducing the test application time of boundary scan boards using multiple boundary scan paths. The test application time that can be achieved with this technique is compared with test application times for boards with a single boundary-scan path. It is pointed out that the test application time reduction depends on the board organization characteristics, specifically on the distribution of chips into groups. The proposed approach has also the potential for

reducing the test evaluation times (i.e. fault detection and isolation) by taking advantage of the parallel test-response of many identical chips. The analytical results obtained were applied to a real board design used for demonstration purposes. The test application time speed-up was found to be consistent with the claims of the proposed approach and almost linearly dependent on the number of scan paths used. It is further suggested that the best approach to chip grouping in multiple boundary scan paths is to maximize the average number of chips per group.

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Dr. Kanopoulos is a member of the organizing committee of the IEEE BIST Workshop, Co-Founder and Chairman of the Program Committee of the IEEE Rapid System Prototyping Workshop, and was a member of the Program Committees of the Government Microcircuit Applications Conference (1988 and 1989). He is a member of the Editorial Board of the *IEEE Transactions on VLSI Systems* and *IEEE Transactions on Computers*. His publications include numerous papers, two book chapters, and the book *GaAs Digital Integrated circuits: A systems Perspective* (Prentice-Hall 1989). He is a member of Tau Beta Pi, Eta Kappa Nu, and the Technical Chamber of Greece.