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The Medium Access Controller of a Customer Premises Network

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Abstract: **This paper presents the architecture of an ATM controller for a Customer Premises Network (CPN). The controller has been designed to implement the cell assembly/disassembly following the B-ISDN ATM layer functionality and the specific requirements of the medium access protocol used in the Buffer Insertion Cell-based LAN. The controller has been implemented using a commercially available FPGA and operates with a 25-MHz clock. The controller's architecture has been based on five operational modules integrated in a single chip and its processing capability is 1.88Mcell/sec. That makes the controller appropriate for use in high-speed applications, like in ATM LANs, CPNs in business and factory environments etc.**

I. INTRODUCTION

The Broadband-ISDN's major goal is to provide a worldwide communication network for efficiently and cost-effectively handling all types of services [1]. This network must be service independent, efficient in the use of the available bandwidth, adaptable to new needs and must be able to interconnect heterogeneous existing networks [2]. In the subscriber/customer site, a special type of network must be used for providing local switching to the internal traffic and a single interface for accessing the B-ISDN services. This network, usually called Customer Premises Network (CPN), can be very simple or extensive enough depending on the customer needs. The customer environment can be classified as residential, business, factory or specialized (like military). Each type of CPN has different service requirements like bit rate, error performance, throughput etc, and different structural requirements like flexibility, expandability, interworking etc.

The B-ISDN uses the Asynchronous Transfer Mode (ATM) which is based on switching or relaying fixed length cells. The ATM is used also in the CPN environment since the fixed cell length and the simplicity of the basic algorithm for forwarding ATM cells make its hardware implementation simple and cost effective [3]. CPN that uses ATM technology is capable of meeting the requirements of different services, supports constant and variable bit rate services, handles the required bandwidth effectively and the resulting dispersed switching allows the establishment of an open architecture.

In this paper, the medium access controller of a CPN is described. The CPN medium access technique is based on the protocol used in the Buffer Insertion Cell-based LAN (BIC-LAN) described in [4]. The used access method is applicable in ring topologies for supporting various types of traffic using cells in a slotted operation with 'destination release'. The method incorporates a distributed algorithm for allocating the bandwidth to the various nodes by comparing the total requested bandwidth to the actually measured traffic and adjusting the offered load accordingly. The access method ensures the transmission of different types of traffic by fulfilling their Quality of Service (QOS) requirements in terms of transmission delay variations and cell rejection rate. The controller has been designed to implement the cell assembly/disassembly following the B-ISDN ATM layer functionality and the specific requirements of the used medium access protocol. The controller consists of five operational blocks:the Transmit direction Fast Transfer (TFT), the Transmit Cell Provider (TCP), the Receive Cell Filter (RCF), the Receive Fast Transfer (RFT) and the Decision Unit (DU). The TFT and TCP are used for servicing the various CPN terminals and for cell assembly while the RCF and RFT filter the incoming traffic, disassemble the received cells and provide the cell payload to the respective terminal. The Decision Unit implements the basic functions of the medium access mechanism and controls the functionality of the other four operational blocks.

Section II describes the used medium access protocol and highlights the architecture of a CPN node as well as the architecture of the UNI-CPN equipment. In Section III the structure of the ATM controller is described in details, emphasizing on how cell processing is performed in high transmission speeds and how multiple terminal adapters are handled. Finally, Section IV concludes this presentation.

II. THE CPN ARCHITECTURE AND ITS COMPONENTS

The BIC-CPN has been developed mainly to support the business environment, which means that various terminal equipment (TE) are concentrated in various locations, a large portion of the generated traffic belongs to internal communications and the supported traffic can be characterized as of interactive type. As it is shown in Fig. 1, the CPN is organised in two levels, the first level concentrates a number of TEs to a CPNode using direct connections and various CPNodes are interconnected by point-to-point links to form a physical ring. One of the ring nodes, the UNI CPNode, is used for connecting the CPN to B-ISDN standard interface link, the T_b interface, following the SDH STM-1 format.

The CPN Access protocol.

The BIC access method has been based on the buffer insertion technique. Idle cells are used to insert new data in the cell stream or for decoupling the differences in the transmission spee

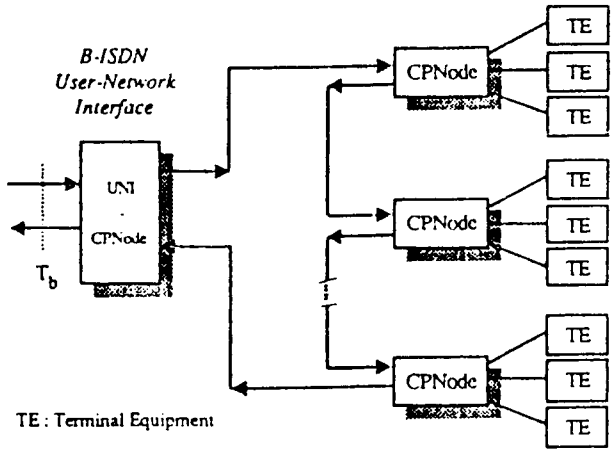

Fig. 1. The Customer Premises Network Architecture.

between adjacent nodes. Each CPNode receives the upstream traffic, rejects the idle and error cells, removes the cells destined to it and transmits its own cells if there are no upstream cells in its ring buffer. Using various network statistics the access method determines if a station cell will be transmitted or the station must defer. The multiplexing of the various CPNode services is performed by the access method using the QOS parameters determined during each service connection establishment. The basic advantages of the BIC access method are its ability to allocate a portion of the available bandwidth to a specific service, like the high priority services, by using a distributed algorithm to keep the total offered load to a target value. This is achieved by controlling the flow of high priority cells using the initially negotiated values and by reducing the traffic of the low priority cells to the currently available bandwidth.

The offered-load control algorithm used in the BIC access method is based on traffic monitoring and is fully distributed since each station decides on its offered load independently from the other stations by using its traffic monitoring statistics. The UNI-CPNode handles the VCI/VPI values associated with the B-ISDN and sets the internal VCI/VPI values for information exchange between CPN terminal equipment (TEs). For medium access protocol purposes, each CPNode has a dedicated VCI/VPI value associating the specific node with its own address for transmitting cells recognizable from all the other nodes. As it will be shown in the next paragraph, this is required for updating in each node the traffic status of each independent node.

When a new connection has to be established, the CPNode estimates the requested mean cell rate generated by the specific service and if there is available bandwidth the connection is accepted. Otherwise, the connection is rejected since there is no available bandwidth to support the specific service effectively. If the connection is accepted, the node transmits a control cell with its dedicated VCI/VPI. This control cell passes through all of the network nodes, so each node is informed about the new status of the traffic connections. The same procedure is used when a connection is released and all nodes are informed about the value of the new available bandwidth. Using this mechanism, all nodes utilize the same protocol parameters and the protocol fairness is guaranteed. The way the TEs of the same CPNode are serviced depends on their priority. In the same priority level the round-robin scheme is used, while the non-preemptive discipline is under consideration for different priorities, but no decision has been made up to now.

The CPNode Architecture

The block diagram of the CPNode architecture is shown in Fig. 2. The ATM layer performs the BIC access protocol functions and provides the multiplexing/demultiplexing of the cells of various connections into the network cell stream. The ATM receives the payload of each cell from the respective terminal adapter (TA) and transmits it into the network by adding its header. The cell headers are constructed using the information provided by the Node Management Unit (NMU). The ATM layer interfaces with the NMU and the various TAs using an Internal Bus which is composed of two high speed (100 Mbyte/sec) data transfer paths (one for cell transmission and the other for cell reception) and a control bus. The control bus operates under the supervision of NMU. The ATM layer contains two 32-bit wide FIFOs for temporary cell payload storage during cell header processing in the ATM layer. The 'X' multiplexer interconnects the two FIFOs when the ATM Controller detects that the cell just received from the network has to be retransmitted into the network or when the cell of a TA must be transmitted to another TA connected to the same node. The ATM layer provides also a link to the NMU for monitoring the physical layer functions. In each direction the ATM layer uses two parallel buses for exchanging information with the Physical layer. A 32-bit bus is used for the cell payload and an 8-bit bus for the cell header. In the transmit direction the header of a cell is transferred to the Physical layer during the transmission of the payload of the previous cell. In the receive direction, the cell header is transmitted from the Physical layer to the ATM layer simultaneously with the first four cycles of the cell payload reception.

A part of the Physical Layer is based on the Fibre Channel architecture. It uses the FC-0 functions of the Fibre Channel (transmission media adaptation, transmitters, receivers and their interfaces) and a combination of the 8B/10B and 4B1C transmission codes [5]. The Physical layer uses some of the FC-1 functions, bit and Transmission-Word boundary synchronization and also contains the required functionality for adapting the ATM cells (idle and information) to the Fibre Channel Datagrams. As a Fibre Channel Datagram is considered the information (number of cells) contained between two idle cells. Each idle

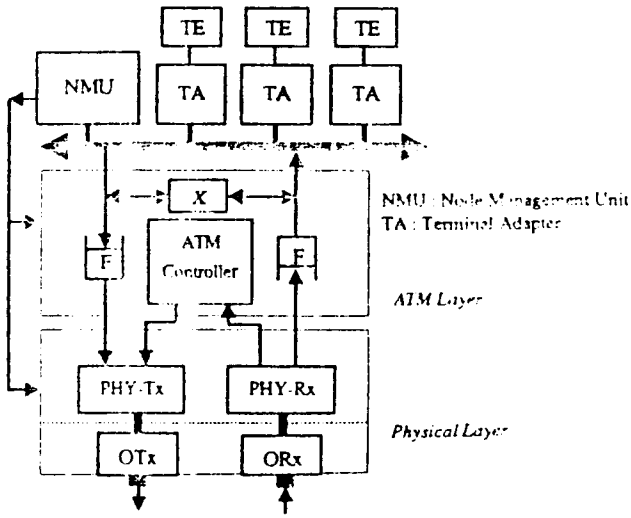

Fig. 2. The Customer Premises Node (CPNode) Architecture.

cell is used simultaneously as the End Delimiter of the current datagram and as the Start Delimiter of the next datagram. The length of a datagram may vary between zero (two consecutive idle cells) and a maximum number of cells determined by the used cell rate decoupling parameter. The Datagrams are reconstructed when they pass through a CPNode and new frame delimiters are generated while the contained data (cell burst) are modified. This modification may include idle cell substitution with node cells or the insertion of idle cells for supplementing the used 'destination release' scheme at the ATM layer.

In the transmit direction the Physical layer accepts complete cells from the ATM and generates the fifth byte (Header Check Sequence-HEC) of the cell header. Then the cell is passed through the Fibre Channel Framer (indicated as the OTx block in Fig. 2) module which generates the appropriate FC frame format and multiplexes the ATM cells in its structure. The FC Framer uses a TAXI transmitter for interfacing the physical medium. At the receiving side, a TAXI receiver accepts encoded serial data and generates encoded parallel data to the receive part of the FC Framer (ORx block). The FC Framer recognizes the data semantics, removes the FC delimiters and regenerates the ATM cells. The PHY-Rx validates the HEC field of each cell header. Single-bit error correction is performed at the header and the cells are passed to the ATM layer for further processing. In the receive direction, the ATM controller scans the header of each received cell and if it is destined to a TE connected to this CPNode, starts the procedure for delivering the cell payload to the respective TA. If the cell does not belong to this CPNode, its payload is transmitted to the Tx FIFO and the cell's header is passed to the controller's transmit section using an internal FIFO. The CPN internal transmission speed is 800 Mbit/sec using optical interface with multimode fibers.

The UNI - CPNode Architecture

The architecture of the UNI-CPNode is given in Fig. 3. A part of the structure of such a node is identical with the one previously described but, instead of the various TAs, the User Network Interface of B-ISDN with the required UNI buffers is connected to the Internal Bus. The UNI interface has been based on the ATM/SDH transmission format (STM-1) [6]. The B-ISDN ATM

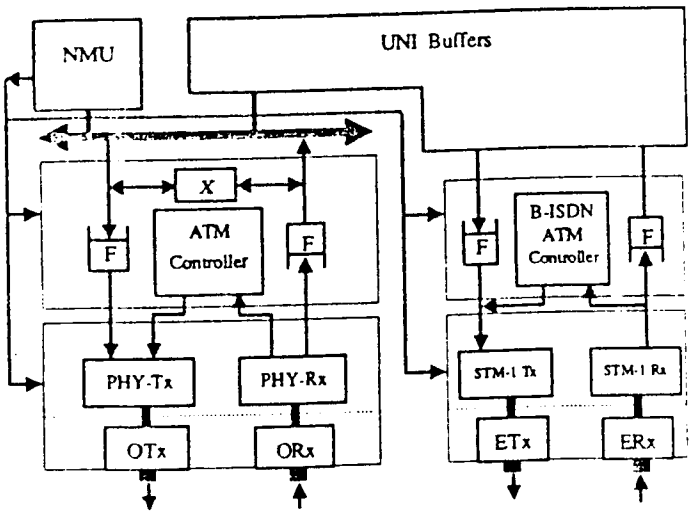

Fig. 3. The UNI - CPNode Architecture.

Controller used in this interface is the same with the one used in the CPNodes with the following modifications: the section of the medium access protocol has been deactivated, the FIFOs are 16-bit wide, there is no bus multiplexing circuit and unassigned cells are used at the ATM layer. At the Physical layer the standard electrical interface is used and the transmission speed is 155.52 Mbits/sec.

III. The Medium Access Controller

As it is shown in Fig. 2, the ATM layer of a CPNode consists of the ATM controller, two FIFOs for cell payload storage and a bus multiplexer for cell retransmission into the network. The used Internal Bus for interfacing the ATM layer with the NMU and the various TAs is initially described. Further, the medium access controller structure is described and various timing diagrams highlight the controller performance.

The Internal Bus

The data transfer rate in the bus is 100 Mbyte/sec and two independent data paths, one for cell transmission and the other for cell reception are used. There is also a Control Bus which is used by the Node Management Unit (NMU) to control the functionality of the various Terminal Adapters (TA), to update the information used by the ATM controller for cell header generation and filtering and for controlling and measuring the performance of the station optical link. The TxBus and the RxBus have similar functionality and use 32-bit wide data buses. Due to the constant length data transfers, there is no typical address bus in these sub-buses but they use a 'board selection' utility in relation with a number of read/write cycles for transfering a cell payload. The TAs use some indication lines for reporting to the ATM controller their availability for data transfer. During each data transfer cycle, the clock generated by the ATM board is used to coordinate the data transfer and no interlocked handshaking signals are used. The Control bus has been developed using the philosophy of the Synchronous Peripheral Interface (SPI) of Motorola Inc. The TA boards are connected in a daisy-chain configuration to form an SPI loop. Two other SPI loops are used for interfacing the ATM and the Physical layer SPI slave modules.

The Controller Structure

The controller's block diagram is shown in Fig. 4. The controller consists of five operational blocks for performing the cell assembly/disassembly and the cell retransmission function. The controller is initialized by the NMU via the SPI interface, which is also used for operational parameters update and traffic statistics collection. The controller operational blocks are the following:

i) The Decision Unit (DU)
ii) The Transmit direction Fast Transfer Unit (TFT)
iii) The Transmit Cell Provider Unit (TCP),
iv) The Receive Cell Filter Unit (RCF) and
v) The Receive direction Fast Transfer Unit (RFT).

The controller's central unit is the Decision Unit, which determines how the various TAs are served, redirects the cell headers to the transmit direction when a cell has to be transmitted back to the network and synchronizes the transmit and receive modules when cell bypassing is performed. When there is available space in the Tx FIFO, the TA Scanning Selector determines which is the next TA that has to be served. The TA Scanning Selector receives a

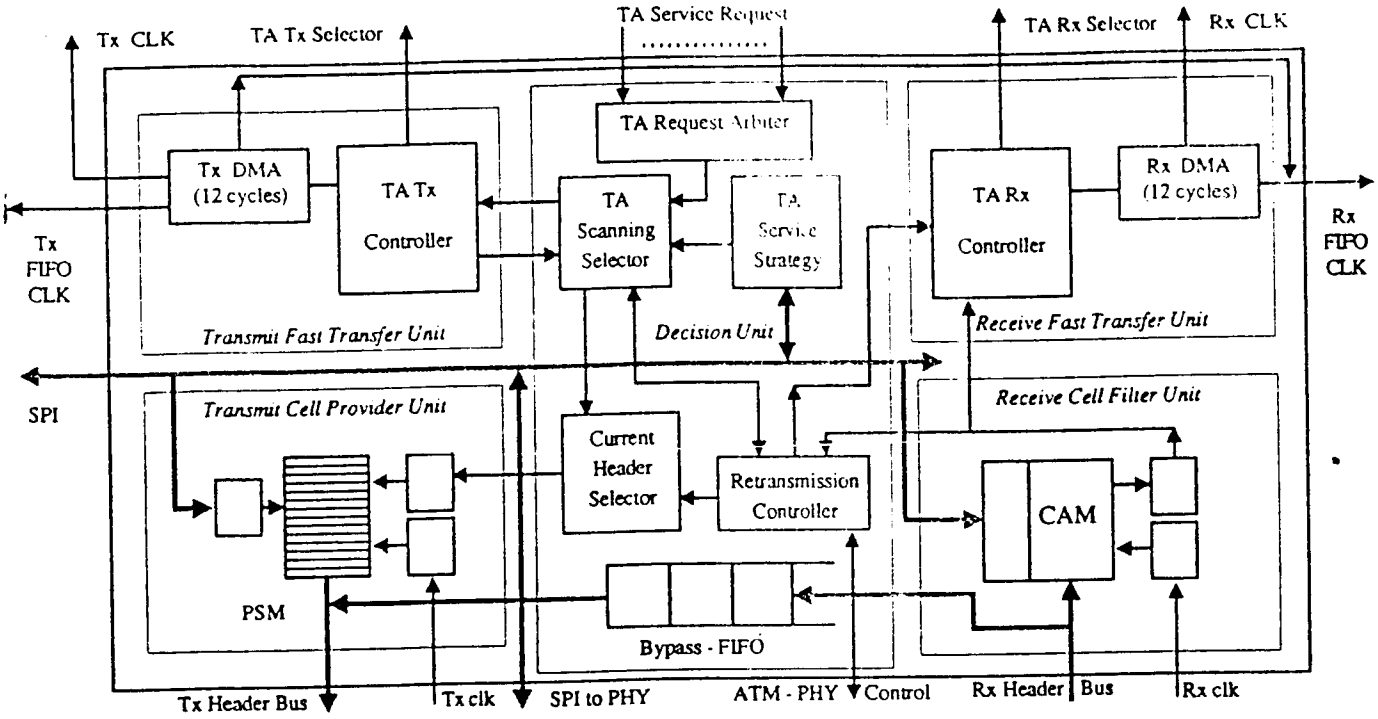

Fig. 4. The Medium Access Controller Block Diagram.

signal from the Retransmission Controller to determine if a cell retransmission must be performed. If no retransmission is necessary, the status of the TA Service Strategy unit and the output of the TA Request Arbiter determine the TA that must be served. The TA Request Arbiter receives a signal from each TA indicating the availability of a cell. The TA Service Strategy is controlled by the NMU which determines the priority of each TA. The developed modules support up to 8 TAs in each CPNode. Fig. 5 shows the timing diagram of a cell assembly and transmision into the network. The decision of the TA Scanning Selector is passed to the TA Tx controller. The previously described decision is made during the payload transmission of the previous cell and no time elapses between the FIFO availability and the new cell reception. When the TXEN signal is asserted a cell payload is transfered from the TA indicated by the TXSEL [2:0] value. The TXSEL [2:0] is generated by the TA Tx Controller and has duration equal to twelve cycles of the TxCLK. The Tx DMA, a fixed length DMA with no address bus signals, generates the required signals to synchronize the TAs with the ATM Tx FIFO. After the completion of the DMA cycle, the cell is ready for transmission to the Physical layer. During this DMA transmission, the TA Scanning Selector informs the Current Header Selector for the position of the associated header in the Position Selectable Memory (PSM). The PSM memory is a special purpose RAM with the following functionality: the length of the memory is 32 bytes, organized in 8 block of 4-bytes. Each block contains the first four bytes of a cell header. For each TA, its position in the Internal Bus is the same with the position of its header in the PSM. The content of each block is updated by the NMU via the SPI when a new connection is established. The PSM output address is determined by combining the respective block pointer and the output of a 2-bit counter which increases when a new TXH-CLK is applied. As can be seen from Fig. 5, when a cell payload is transmitted from ATM to the Physical layer, the transmission of the header of the next cell is performed in parallel to the last four cycles via the Tx Header Bus (TXH[7:0]). In Fig. 5, during the transmission of an idle cell by the Physical layer (T_Bus in High-Z state), the payload of a cell from TA#3 is stored in the ATM FIFO and its header is transmitted to the Physical layer. When the cell payload of TA#3 is transmitted to the Physical layer, the TA#4 is serviced and the TA#4 connection header is generated. Following this parallel information flow in the ATM layer, an 1.88 Mcell/sec processing speed has been achieved in the ATM layer. The circuit operational speed is 25 MHz and it has been implented in a XC4005 FPGA of XILINX Inc.

In the receive direction, a parallel architecture is also used. As it is described in [5], the four first bytes of a cell header are received in the ATM layer concurrently with the first four 32-bit blocks of the cell payload. The cell header is stored in parallel in the Bypass-FIFO of the Decision Unit and the content of their VCI/VPI is compared in the Content Addressable Memory (CAM) of the Receive Cell Filter Unit. The CAM memory contains the VCI/VPI values of each TA and generates this value each time a match is detected. In this case, the cell is destined to a TA in this node and must be removed from the network traffic. This cell header is deleted from the Bypass-FIFO and the TA Rx Controller is informed about the destination of the current cell. Fig. 6 shows the timing diagram of a cell reception. The RXH-CLK indicates the cell header reception, the payload is stored in the FIFO using the R_BUS[31:0] and when the TA Rx Controller receives the value of the destination TA, generates the RXSEL[2:0] signals to determine in the Internal Bus the respective TA and by using the RXEN and RXCLK signals transmits the payload. The content of the CAM memory is updated by the NMU using the SPI interface. Both the PSM and CAM memory modules are used for providing a direct relation between the static TA board position in the Internal Bus with the dynamic allocation of the VCI/VPI values in the ATM layer.

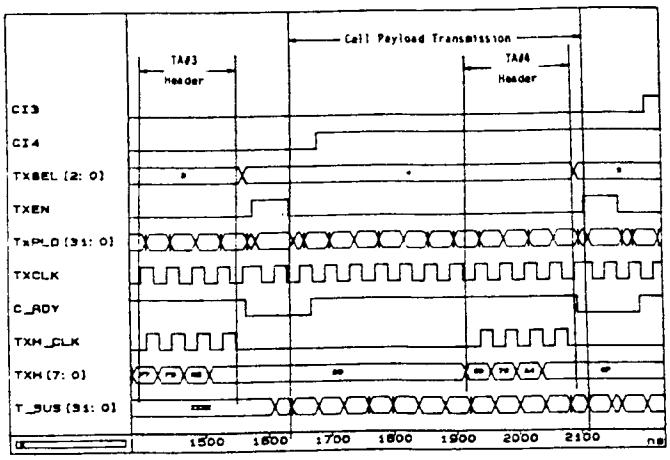

Fig. 5. Cell assembly timing diagram.

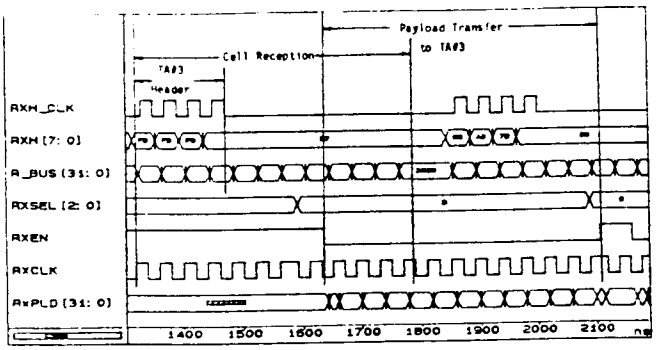

Fig. 6. Cell disassembly timing diagram.

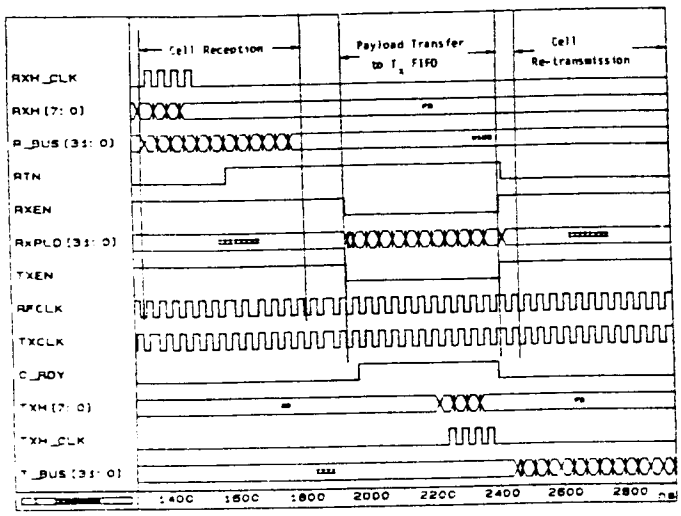

Fig. 7. Cell retransmission timing diagram.

The retransmission of a cell back to the network is shown in Fig. 7. When the CAM memory decides that the received cell header does not match with its prestored values, signals the Retransmission Controller to not allow the Physical layer to generate an idle cell until the cell has been retransmitted. The Retransmission Controller forces the TA Scanning Selector to seize the service of the next TA and gives the highest priority to the retransmission procedure. In this case the Rx DMA is deactivated by the TA Rx Controller and the control of the transfer from the Rx FIFO to the Tx FIFO is performed by the Tx DMA and the TA Tx Controller, which is also responsible for activating the ATM multiplexer for interconnecting the receive and transmit data paths of the Internal Bus. The RTN signal indicates that a retransmission process is in progress. During the cell payload transfer from the Rx FIFO to the Tx FIFO (RXEN, TXEN asserted) the cell header is transfered from the Bypass-FIFO to the Physical layer (TXH-CLK).

IV. Conclusion

In this paper, the Medium Access Controller of a Customer Premises Network (CPN) has been described. The CPN is used to interconnect customer terminals, to provide fair access to the available network bandwidth and to allow them to share a B-ISDN UNI interface. The CPN operates in 800 Mbit/sec internally and its access protocol uses fixed length cells in slotted operation with a destination release method and supports various types of traffic.

The Medium Access Controller implements the basic functions of the ATM Layer by using the services of the Physical Layer and supports various types of TA entities. The controller also implements the specific functions, like cell retransmission and destination release, required by the used medium access protocol. The Medium Access Controller has been implemented using a XC4005 Field Programmable Gate Array (FPGA) of XILINX. The performance results of the experimental prototype show that its processing capability satisfies the predetermined requirements and is measured to be 1.88 Mcells/sec.

Acknowledgment

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