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Simulation Analysis of Access Protocol Storage Requirements in a Local Area Network Node Environment

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SIMULATION ANALYSIS OF ACCESS PROTOCOL STORAGE REQUIREMENTS IN A LOCAL AREA NETWORK NODE ENVIRONMENT

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Abstract: Nodal storage limitations in a store-and-forward computer network lead to blocking; moreover in high-speed LANs where time restrictions are critical, they result in degradation of network performance due to loss or retransmission of blocked packets. In this work we consider the Input/Output Packet Buffer (I/O PB) at the interface between the Medium Access Control (MAC) unit, responsible for the access protocol, and the Bursty Data Module (BDM), responsible for the processing of higher layer protocols. The arrival of packets to the buffer from the MAC follows an interrupted procedure with exponential distribution for the busy and idle times. The arrival interruptions originate from the Access Protocol used for a high speed (144 Mb/s) Integrated Services LAN. Both busy and idle times are expressed in clock time periods with reference to the network speed. The server which represents the interface between the I/O PB and the BDM is also available in interrupt form to idle times. The measured performance for the delay contribution and the buffer size through simulation analysis is also presented in this paper. Finally, a comparison between the implementation and the simulation is carried out allowing the optimum choice of the buffer design parameters through a trade off between the required performance and the hardware implementation.

I. INTRODUCTION

The analysis of the buffer and storage facilities in a network node environment has attracted the attention of a large number of studies because it is often one of the critical resource problems. Many authors have dealt with the study of buffer systems using a number of assumptions for their analysis either concerning the size of the buffer or the type of the arrivals and the servers available to the buffer [1],[2]. Usually the generalized approaches, appearing in the literature, suffer from two major problems:

i) They consider arrival and departure processes which only approximate the practical system and the used implementation techniques.

ii) It is considered that the transfer of data at the input of the buffer and the evacuation of the buffer are "instantaneous". This fact in some cases, especially for high speed Local Area Networks, is not true because usually the data transfer process becomes an important factor of the buffer performance.

The analysis presented in this paper originates from the study and implementation of the input/output (I/O) buffer for an Integrated Services Local Area Network (ISLAN) [3]. The I/O buffer in the node structure lies between the module which is responsible for the processing of packets for the communication protocols, from the Data Link Layer up to the Transport Layer, and the module which is responsible for the implementation of the Access Protocol. The Access Protocol module implements a Hybrid Protocol and delivers/accepts packets to/from the buffer following an interrupted Poisson process using a high-speed parallel interface [4],[5],[6]. The buffer delivers/accepts packets to/from the BDM, through a high speed VMX bus, following an interrupted exponential process.

The paper addresses the analysis of the I/O buffer of a node for the Local Integrated Optical Network (LION) currently implemented under the partial financial support of the Commission of the European Communities within the context of the ESPRIT program.

Section II presents the functional block diagram and the critical design/performance parameters of the I/O buffer as well as the details of the buffer interfaces. In Section III the simulation performance analysis of the I/O buffer is presented and finally Section IV presents the discussion of the results obtained in Section III.

II. THE I/O PACKET BUFFER (I/O PB)

In Fig.1 the functional block diagram of the I/O PB is depicted. The I/O PB interfaces with the Access Control Manager (ACM), which is responsible for the access protocol implementation, uses two parallel 8-bit buses and the required control signals, one for the Read and one for the Write direction, respectively. The interface speed of 18 Mbytes/sec as well as the 8-bit format are set by the ACM structure.

The I/O PB follows a pipeline pair structure in order to achieve the required high operation speed and the data flow speed adaptation. During the Read channel operation after the ACM notification of the existence of a packet for delivery, the packet is transfered to the Read FIFO Buffer (RFB) under the control of the Read Interface Controller (RIC). After the packet storage the actual length of the packet has been calculated and it is checked with the packet length indicated in the first two bytes of the packet. Then, if the calculated and indicated packet lengths are not the same, the packet is deleted from the RFB otherwise it is kept for further processing. In this way, on the one hand we consume less buffer space and on the other hand we offload both the processing inside the I/O PB and BDM and the VMX bus utilization.

Then, for the valid packets of the RFB, the Frame Check Sequence Generation and Validation (FGV) unit is requested. After FGV acquisition and the indication of a valid packet, the VMX Interface Handler (VHI) requests the VMX bus through an interrupt structure for packet transfer. The FGV operation speed is 8, 16, or 32 (byte, word, longword transfer) times the VMX transfer rate because it is implemented in a serial form.

During the Write channel operation the interface towards the ACM follows the speed and form described in the Read channel operation. In addition the Access Protocol permits a maximum of four packets to be transmitted per node access, therefore the size of the Write FIFO Buffer (WFB) is four times the maximum packet length. The transfer to the ACM is under the control of the Write Interface Controller (WIC). When there are not four packets in the WFB then the WIC through the VIH generates an interrupt to the BDM for a transfer of a packet to the WFB. Then the WIC requests the FGV for the FCS sequence generation following the CCITT-32 FCS standard.

In the FGV acquisition and the VMX interrupt generation processes the Read operation has higher priority from the Write operation.

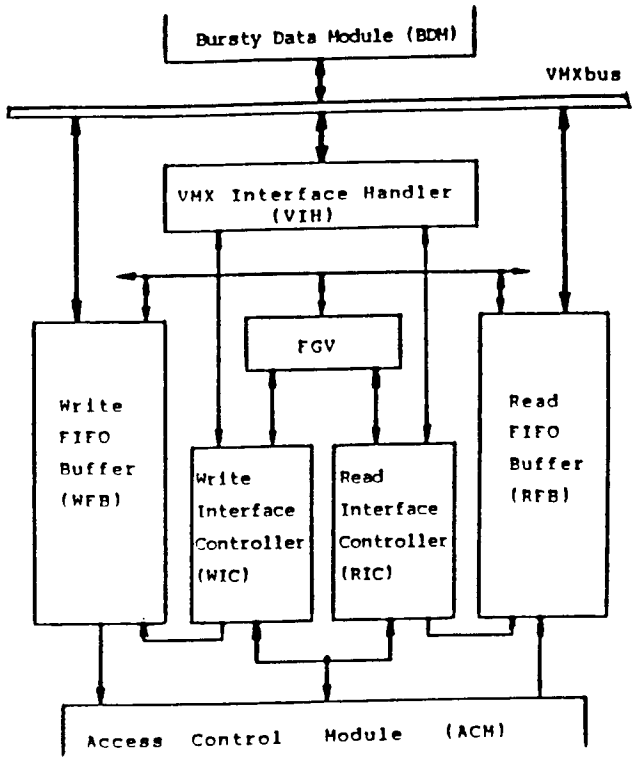

Fig.1. The functional diagram of the I/O Packet Buffer.

For the VMX interface transfers a DMA controller is foreseen with a target speed of 4 Mbytes/sec. The DMA controller is under the control of the BDM which is also responsible for the higher level protocols processing and the users interface [3], [7]. Therefore, for the interrupt handling procedure congestion problem, the I/O PB has one of the highest priorities in the interrupt handling routines supplied by the BDM for the VMX and the BDM internal functions.

The transfers at the two I/O PB interfaces (ACM and BDM) are asynchronous, moreover for each individual interface the transfers of the Write and Read channels are also asynchronous and independent to each other. Therefore, a structure which permits independent and parallel processing of the received and transmitted packets at each interface will speed up the I/O PB function. In addition, at the I/O PB-BDM interface, since the BDM is involved in a large number of processing functions, it is required to offload the handshaking procedures between BDM and the RB, because the VMX interface is not always available for the I/O PB transfers. Therefore, the Write Input Buffer (WIB) and the Read Output Buffer (ROB) are added.

IV. THE SIMULATION PERFORMANCE ANALYSIS OF THE I/O PB.

The simulation model for the I/O PB [8] is shown in Fig.2 and has the following characteristics:

i) The size of the RFB is assumed infinite.

ii) The size of the WFB is four packets.

iii) The VMX bus acquisition from the Read, Write channels and the BDM follows an interrupt procedure where the Read channel has the highest priority and the BDM the lowest. Moreover, the VMXbus is released through a "Release When Done" procedure, therefore when the Read channel, or the Write channel, or the BDM acquires the Bus, any further request is serviced after completion of the work of the current user, following the priority scheme previously mentioned.

iv) The request procedure of the VMX bus for the BDM follows an exponential distribution indicated by busy times (when the BDM requires the VMX) and idle times (when the BDM does not require the VMX) exponentially distributed.

v) For the ACM interface, regarding the Read channel it is considered a busy time period (packets received) and an idle period (no packets received), both exponentially distributed. The same holds for the Write channel, for packets transmission.

vi) The ROB and the WIB are both one packet long.

vii) The operational speeds of the FGV and DMA controler are programmable.

The measured quantities of the I/O PB are:

i) The mean and maximum values of the RFB and WFB.

ii) The mean delay for received and transmitted packets (queueing and transmission delay).

iii) The FGV utilization by the Read and Write channels.

iv) The VMX utilization by the I/O PB and the BDM.

v) The number of transmitted and received packets.

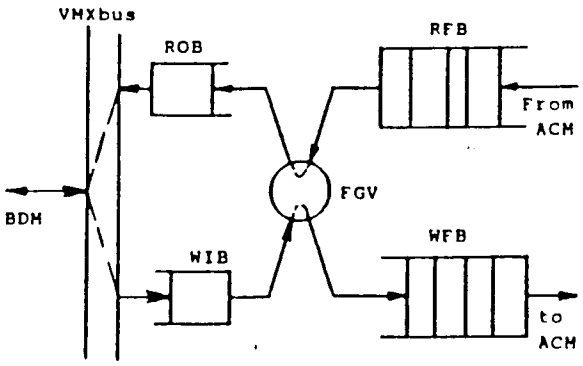

Fig.2. The simulation model.

The traffic scenario used for the simulation of I/O PB is based on a previous analysis of the hybrid protocol [4] and on the models used in the literature [8], [9] which consider that a node in a network receives twice the traffic that delivers to the network. Considering the LION network [3], [4],[7] for a frame of 5 msec, a network speed of 144 Mb/s and 300 nodes, the reference mean arrival rate for the Read channel is calculated 200 packets/s. The simulation runs for arrival rates between 25 packets to be received and about 200 packets to be transmitted (write channel) for valid simulation results. The network is considered in steady-state which means that the BDM has packets to transmit and the network has packets to deliver to the nodes. The reference time is the hybrid frame and the distribution of the availability of the VMX for transfers between the BDM and I/O PB is taken 40%, 60% and 80% of the hybrid frame duration.

The DMA speeds used are related to the organization of the tranfers and it is 2 MWords/s or 2 MLongwords/s for 16 bit and 32 bit transfers, respectively.

In Fig.3 the throughput-delay performance of the Read channel is presented for the following cases:

	DMA speed	VMX availability
a	2ML	80%
b	2MW	80%
c	2ML	40%
d	2MW	40%

For the above cases the measured FGV utilization was always less than 10% for the Read channel and its contribution to the total delay was less than 250 μsec for a FGV operational speed of 80 Mb/s which is always less than 5% of the total delay. Then the major part of the delay as it is observed in Fig.3 is due to the VMX availability and the DMA speed contribution to the delay is a secondary factor. Taking as a reference the curve "a", the variation of the delay due to the decrease of the DMA speed (curve "b") is much less than the variation of the delay due to the decrease of the VMX availability (curve "c").

In Fig.4 and Fig.5 the Mean Read Buffer and the Maximum Read Buffer sizes are shown respectively for the cases used in Fig.3. From these figures it is observed that the contribution of the DMA speed and the VMX availability is equivalent (comparing curves "b" and "c" with the curve "a") as far as the

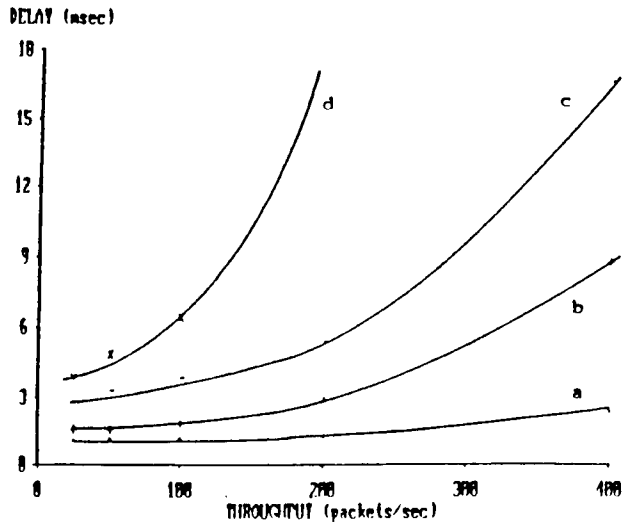

Fig.3. The Read channel Throughput-Delay characteristics.

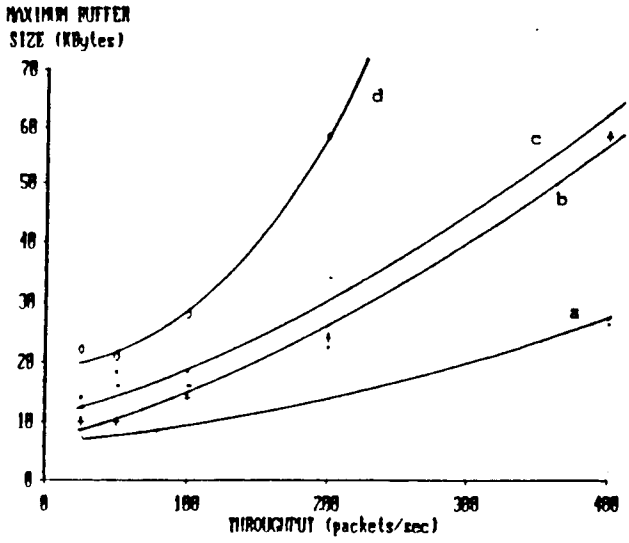

Fig.5. The Read FIFO buffer maximum length.

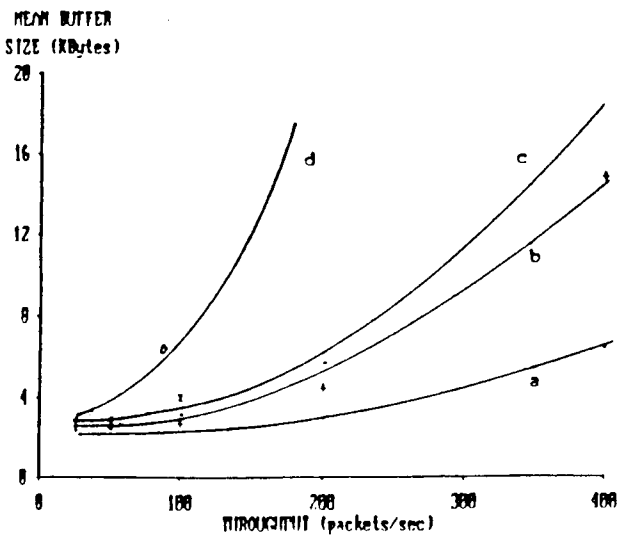

Fig.4. The Read FIFO buffer mean length.

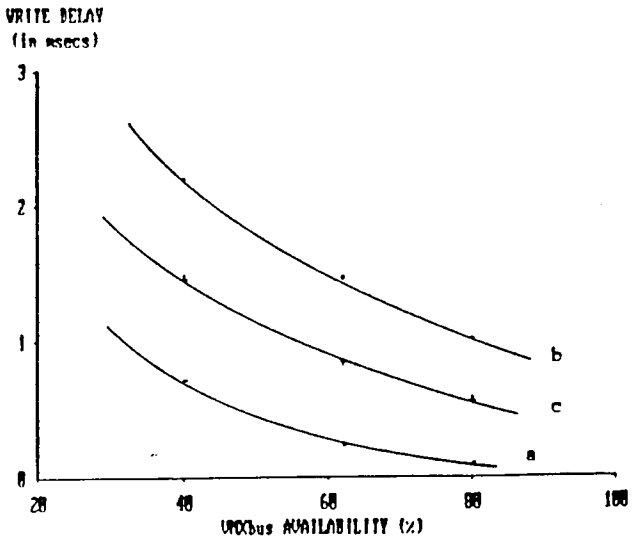

Fig.6. The Write channel Delay characteristics.

buffer size is concerned.

In Fig.6 the Write channel delay is shown versus the VMX bus availability. The delay for the Write channel is measured from the time where the Write channel requests a packet from the BDM until the packet is stored at the WFB. The following curves are depicted:

i) a: considers the contribution of the VMX bus availability only to the delay.

ii) b,c: the contribution of the VMX bus availability and the DMA speeds for 2 MWords/s and 2 MLongwords/s, respectively.

From Fig.6 it is observed that for low VMX bus availability the contribution of the DMA speed is equivalent to the contribution of the VMX bus availability. For higher VMX bus availability values, the major contribution to the delay originates from the DMA speed.

V. DISCUSSION

From the simulation results for the buffer size (Fig.4,5), we can choose the implementation of the DMA at a speed of 2 MWords/s and the RFB at a size of 32 Kbytes (considering the reference mean arrival rate to be 200 packets/sec). From Figures 4, 5, 6, we can observe that through the use of the WIB and ROB we can give the highest priority for the Read channel in the VMX bus interrupt structure, allowing in this way higher VMX bus availability for the I/O PB taking also into account that only useful information is transfered to the BDM (non valid packets are already rejected internally to the I/O PB).

Finally from the architecture of the I/O PB and the results of Fig.6, we can state that the major contribution in the total packet delay is due to the hybrid protocol [4] and the I/O PB is very efficiently transfering the packets avoiding any bottleneck problems.

VI. ACKNOWLEDGMENTS

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