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Access Control Module for Local Integrated Optical Network

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ACCESS CONTROL MODULE FOR LOCAL INTEGRATED OPTICAL NETWORK

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The implemented access control module (ACM) for a multiservice high-speed network, which performs the access protocol functions, is presented. The operating speed of the module is at 18 Mbyte/s and the protocol delimiter recognition time is 30 ns. The used architecture provides a low cost implementation well suited for the use of custom or semicustom VLSI implementation.

Introduction: The local integrated optical network (LION), ESPRIT project 169, is a multiservice, bus-structured, high speed (144 Mbit/s) optical local area network. LION supports stream traffic like telephony, videoconference, high resolution graphics and packet traffic like low, medium and high speed interactive computer data. The required performance in terms of network efficiency and grade of service offered to each type of traffic promotes the use of a hybrid access protocol (HAP).[1] Under the HAP the digital channel is organised in contiguous periodic frames of 5 ms duration. Each frame consists of two regions, namely the circuit and the packet. Delimiters are used to discriminate the start of frame (SF), the boundary between the two regions (RB) and the end of activity (EA) of a node activity in both regions. In each frame there is one access per network node in the circuit region, while in the packet region may be a variable (integer or not) number of packet rounds. Any interrupted packet round is resumed in the successive frames starting at the point where it was interrupted, therefore a start of round delimiter (SR) is used. The access in both regions follows a dynamic asynchronous time division multiplexing scheme in a round robin procedure based on the physical enumeration of the network nodes and the maximum number N of attached nodes.[1,3] A node which has nothing to transmit does not perform any operation, thus the next higher in order node after a time-out time (TL) accesses the bus. Inside each node activity in the circuit/packet region the circuit channels/packets are distinguished by the start of channel (SC) delimiter. The most up-stream node in the bus is responsible for the frame delimiter generation but actually every node is capable of performing the above, thus providing a fully distributed management of the frame.

Access control module: Each network node communicates with the physical interface, by the medium access unit (MAU) responsible for coding/decoding and synchronisation, through three channels:

(i) the write channel (WC), which is responsible for the circuit and packet data transmission, providing also the HAP delimiters.

(ii) The read channel (RC), which is responsible for the circuit and packet data reception, basically by detecting the HAP delimiters.

(iii) The sense channel (SC) which is responsible for the hybrid frame evolution monitoring by detecting the HAP delimiters, to implement the round robin scheme and to also notify to the WC the access right and finally to inform the node management for any hybrid frame abnormal conditions.

The interface is implemented in parallel form through the use of separate 8 bit buses and control signals for each channel. The interface receives data from MAU at a speed of 18 Mbyte/s, which imposes a maximum permitted decision time of 56 ns. In addition, for reliability purposes the HAP delimiters are using three consecutive bytes for coding and their detection is based on a majority rule (2 of the three bytes must match the required code). Therefore, for the delimiter detection a 'window' of four consecutive bytes has to be monitored each time. In the case of a delimiter existence, three of the 'window' bytes constitute a delimiter event and then a tight synchronisation is required for the reception of the fourth byte. The same synchronisation problems arise in the case of reception, where the fourth 'window' byte belongs to circuit or packet data, because a splitting of the internal ACM bus is required since the data are directed to different processing units. In Fig. 1 the functional details of the implemented ACM as well as the WC, RC and SC internal modules are reported.

The RC after the 4-byte 'window' for the delimiter event recognition uses a 3-byte window for the specific delimiter recognition. For the circuit data the bus is directed to the stream interface while for the packet data further processing is foreseen. In both cases the HAP delimiters are decapsulated. The packet data then, are processed through a 9-byte 'window' for the MAC layer address matching and only packets referred to the current node are directed to the packet data interface after address decapsulation.

The SC unit follows the same architecture as the RC with the task of HAP delimiters recognition for the monitoring of the hybrid frame evolution. In addition SC detects and counts in the two distinguished regions of the hybrid frame the EA and TL delimiters to detect the access right of the node to which it belongs. In this case SC notifies the WC to submit the stream or packet data to the MAU. Another monitoring task is to report to the local management unit of any abnormal conditions detected from the hybrid frame evolution.

The WC after the notification from the SC in both regions delivers the data after the encapsulation of the HAP delimiters

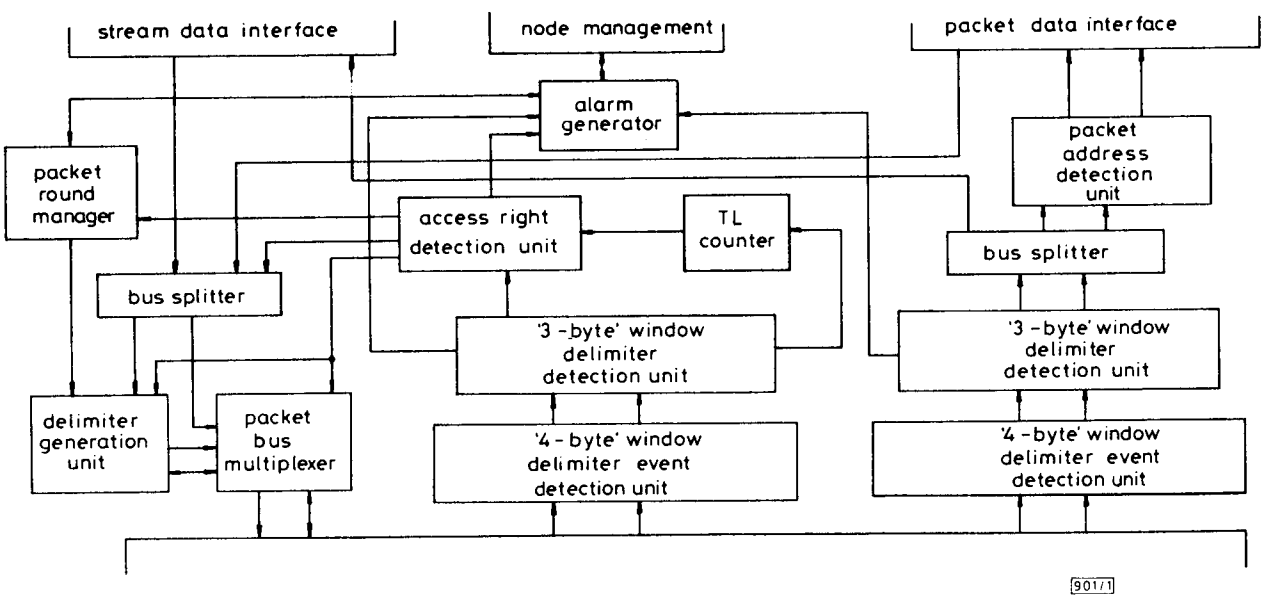

Fig. 1 *Block diagram of ACM*

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at a speed of 18 Mbytes/s. In addition, in the packet region the WC implements the required algorithm from HAP for the maximum number of variable length packets per node access.[3,4] The required performance of the ACM is focused on the speed of the access algorithm implementation and especially the speed of the delimiters recognition by the SC and RC modules, the fast bus splitting and synchronisation of the internal ACM bus, and the fast delivery of data by the WC for better network utilisation.

Experimental results: The implementation approach of the ACM is based on the available state of the art techniques. Three double density Eurocard boards, using wire wrap techniques and LSI and MSI integrated circuits, constitute the prototype implementation which is followed by logic cell array (LCA) implementation. The testing of the prototype is based on a flexible and versatile HAP traffic generator based on a 16 bit CPU and very fast FIFO memories with an operational speed of 20 Mword/s. Fig. 2 presents the timing diagram of the frame delimiter's recognition of HAP pro-

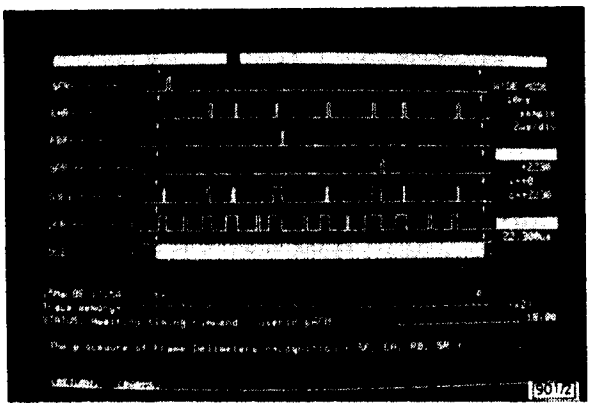

Fig. 2 *Frame delimiter recognition procedure*

cedure with a sampling time of 10 ns/sample. The recognition time for the frame delimiter event is 30 ns and the time required for the detection of a specific delimiter is 44 ns. Finally, Fig. 3 presents the activity of the WC in the packet region for a node which has to transmit 2 packets at the current access. The measured time for the WC to deliver the first byte after the notification by the SC is 38 ns, while for the first stream byte it is 10 ns.

Conclusion: The design and implementation of a high speed access control mechanism for a multiservice LAN is presented. The implementation uses discrete components of the fast TTL family since the operational speed of the system is at

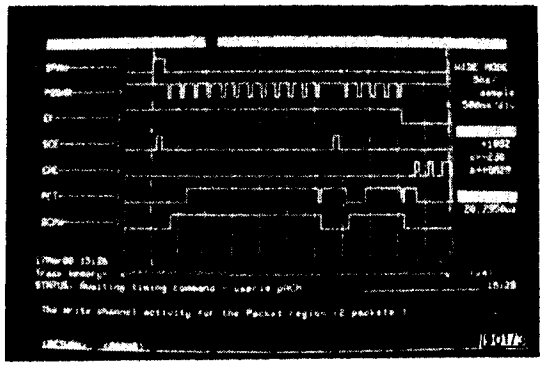

Fig. 3 *Write channel activity*

18 Mbyte/s. The measured time for a delimiter event recognition of the hybrid frame is 30 ns which is very well bound into the byte duration of 56 ns with the duty cycle of 66% and the medium data rate of 144 Mbit/s. The control mechanism also provides a continuous monitoring of the down-stream activity of the network providing alarm signals for the abnormal situations to the network management. The system is totally independent of the structure of the packet and stream data as far as the processing of the communication protocols is concerned and implements in this way the medium access control (MAC) layer functions in absolute conformance with the ISO model for OSI.

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