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A High Speed Access Mechanism for a multiservice LAN at 144 Mbps

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ABSTRACT

A prototype of a high speed access mechanism that performs the required services of the Medium Access Layer (MAC) following the ISO model of OSI, has been implemented and tested. This access mechanism, called Access Control Manager (ACM), is part of the node hardware and software for a multiservide fiber-optics LAN at 144 Mbps. The network traffic includes both stream (circuit switched) traffic and bursty (packet switched) traffic. Therefore a hybrid protocol for the access on the medium is followed based on a Dynamic Asynchronous Time Division Multiplexing (DATDM) scheme. Because of the high speed stream traffic involved, fiber cab le has been chosen as the network carrier following an active bus topology and the carrier speed has been set at 144 Mbps. The Physical Layer at the interface with the ACM provides:

i) An 8-bit bus that carries information and commands (delimiters) of the hybrid protocol at a rate of 18 Mbytes/sec.
ii) A 4-bit bus that carries commands of the hybrid protocol at a rate of 18 Mbytes/sec.
iii) Control signals related to the previous mentioned buses, e.g. strobes, and status signals, that discriminate between command and information data at the buses.

The first part of the ACM, called Sense channel is responsible for the recognition of the hybrid protocol delimiters, the control of the proper evolution of the frame in conjuction with the node manager, and the recognition of the right of access of the node in which it belong. The second part, called Write Channel, is responsible when it is notified from the Sense channel to add the required hybrid protocol delimiters to the bursty data, to multiplex the stream and bursty data and to synchronize the transmission during the required stuffing periods. Finally the third part of the ACM, called Read channel, is responsible to recognize the hybrid protocol commands, to demultiplex the received information to stream and bursty data, to decapsulate the protocol delimiters, and to pass to the upper layers transparently stream data and bursty data that their address matches the address of the node where it belongs.

The ACM has been built using discrete LSI and MSI components (fast TTL family) because of the required high speed of operation. The prototype has been implemented on three Eurocards using wire-wrap techniques.

I. INTRODUCTION

The growing penetration of high bandwidth services, the required sharing of power and resources and finally the development in the area of microelectronics and VLSI fabrication, create the background for the intense interest in the area of the high speed multiservice Local Area Networks (LANs), during the past several years. The large demand for the introduction of new services in conjuction with the traditional voice and data traffic requires new approaches or "integrated" approaches for LAN topology, access method, medium and speed of transmission [1],[2]. The increasing need to integrate different communications in one transport system, without any constraint on the source traffic-carrying capacity [3], is stimulated by the users needs in applications such as:

- office automation, including the extensive use of laser printers, high resolution graphics, Personal computers and videotelephony
- scientific computation
- professional and technical documentation
- computer-aided design for hardware and software development
- videoconferencing
- personnel management
- logistics data interchange
- finance and auditing
- interconnection with several public and private LANs.

The required performance in terms of network efficiency and grade of service offered to each type of traffic in a multiservice LAN promotes the use of fibers as the transmission medium and it also sets the transmission speed over the 100 Mb/s [4].

Since the packet switching concept and the developed access protocols for the bursty traffic cannot guarantee the required performance for applications of the stream type, other than voice the hybrid switching concept appears to be promising solution for the multiservice LANs [5],[6].

In this paper the hybrid switching concept is used to define the access protocol for a multiservice LAN, with a transmission speed of 140 Mb/s, using fiber cables, which covers on average a radius of 10 Kms. The traffic scenario is based on an environment of about 5000 users which requires about 300 nodes and a throughput of about 150 Mb/s for non blocked stream services and 12.5 Mb/s for packet services.

II. THE ACCESS PROTOCOL

The hybrid access protocol for the system under consideration is shown in Fig.1. The digital channel is organised in contiguous periodic frames of a duration of 5 ms. Each frame is constituted by two regions, the circuit and the packet [7],[8].The beginning of a frame is marked by the Start-of-Frame (SF) delimeter and the beginning of the packet region is defined by the Region Boundary (RB) delimeter. Every frame includes one circuit round whereas may include a variable (integer or not) number of packet rounds, which are discriminated by the Start of Round (SR) delimeter. Any interrupted packet round is resumed in the successive frames starting at the point where it was interrupted. The network nodes are numbered in accordance to their physical position on the bus and each node knows the maximum number N of the operating nodes. The access in both regions follows a Dynamic Asynchronous Time Division Multiplexed (DATDM) scheme in a Round Robin procedure.

In the circuit region every channel inside the node activity is assigned a slot of duration proportional to its service bit-rate [9]. In the packet region, the nodes share the spared frame capacity after the servicing of the entire stream traffic of the network nodes, by delivering from one to four packets, in each node per access. The packet length is variable between 256 bytes and 4 Kbytes. During the circuit region activity of each node, each channel beginning is marked with the Start of Channel (SC) delimiter. In the packet region the beginning

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of a packet transmission from a node it is also marked with the SC delimiter. The end of activity for the nodes in both regions is marked by the End-of-Activity (EA) delimiter. A node which has nothing to transmit does not perform any operation, then the next higher in order node after a Time Out Time (TL) accesses the bus. The TL time is defined by the maximum access time (T_a) of a node and the round trip delay for the transmission in the fiber carrier. The frame evolution for a node is monitored from the signals SF,RB,SR and TL. The most up-stream node in the bus is responsible to generate the frame delimeters but actually every node is capable to do it, thus providing a fully distributed management of the frame. The access algorithms for the circuit and packet regions are shown in Fig.2 and Fig.3 respectively.

III. THE ACCESS CONTROL MECHANISM IMPLEMENTATION

The network nodes communicate with the physical interface, the Medium Access Unit (MAU), through three channels:

- The Write channel which is responsible for the circuit and packet data transmission, providing also the access protocol delimeters.
- The Read channel which is responsible for the circuit and packet data reception, by recognizing the frame delimeters.
- The Sense channel which is responsible to monitor the frame evolution by recognizing the frame delimeter and to notify also to the Write channel the beginning of its right of access in each frame region.

The interface of the access mechanism with the MAU is implemented in a parallel form at a speed of 18 Mbytes/s and it constituted by the following:

1. To the Read channel by an 8-bit data-command bus (DCB0-DCB7),a control/strobe signal to distinguish data and command bytes (DCS),and a signal to indicate for every frame if a coding error has occured (CMIEr).
2. To the Sense channel a similar interface as for the Read channel with the exception of a 4-bit command bus (CB2-CB5) because the Sense channel requires the command bytes only, which uses only four bits for the delimtter coding.
3. From the Write channel an 8-bit data-command bus and the strobe signals. The Write channel accepts from the MAU a signal indicating the bit-stuffing periods.

The Read channel, which is totally independent from the two other channels recognizes the normal frame evolution through the frame delimiters. The SF,RB,SR and EA delimiters are structured as 3-bytes for redundancy purposes and the decision is made through a majority rule (2 of 3 bytes required to match the code of a specific delimiter). Therefore the Read channel uses a "window" of four concecutive bytes to recognize the existence of the event frame delimiter and then by the majority rule to detect the specific delimiter. Then the Read channel split the received data to a stream and a packet bus according to the frame region. The stream data are directed to the upper layer interface "transparrently" after the frame delimiters decapsulation. The packet data are further processed through a 9-byte "window" because of the packet structure which is:

1. The first byte is the SC delimiter.
2. The second and third bytes indicate the packet length.
3. The fourth to ninth bytes are the node MAC address.

If the packet is intented for the current node after the delimiter and address bytes decapsulation are delivered to the upper layers for further processing, otherwise they are disregarded.

The Sense channel follows the same structure as the Read channel up to the point of the specific delimiter recognition. Then by counting the EA, TL and RB signal occurences it generates the signals Start of Stream Activity Write (SSAW) and Start of Packet Activity Write (SPAW) to notify to the Write channel, for the current node, the righ of access for the

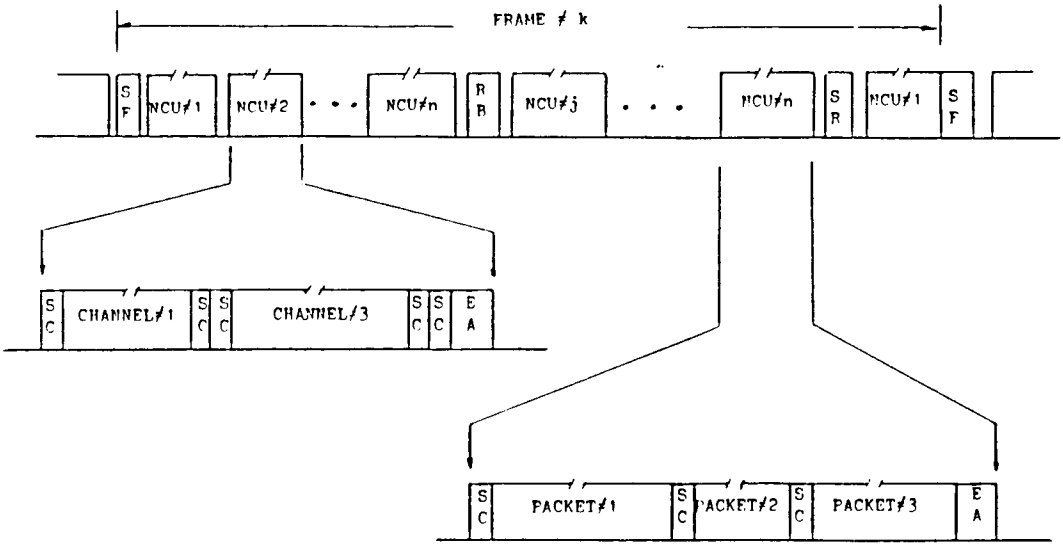

Fig.1. The Hybrid Frame format.

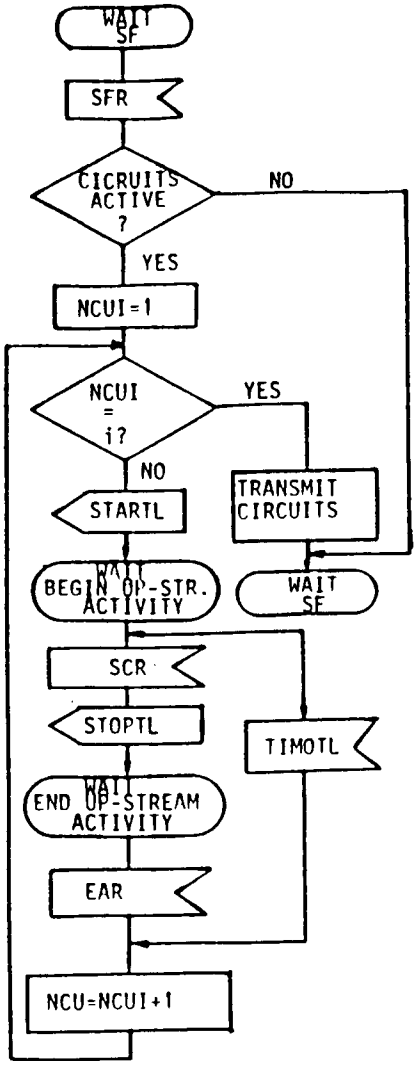

Fig.2. The circuit region access algorithm.

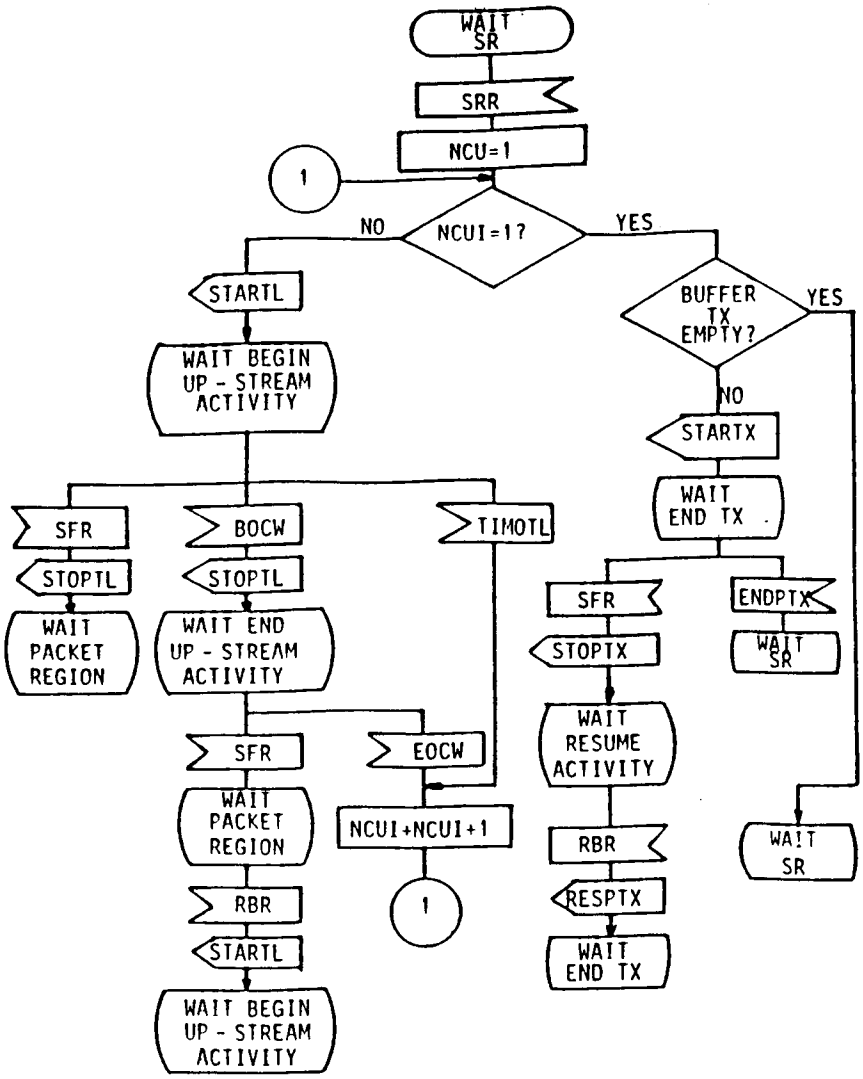

Fig.3. The packet region access algorithm.

circuit and packet regions respectively. The Sense channel also provides the node statistics and alarm signals for the abnormal frame evolution to the node manager.

The Write channel after the reception of the SSAW signal from the Sense channel allocates the bus to the stream data interface and it passes them transparrently. The stream data already include the SC and EA delimiters. When it receives the SPAW signal from the Sense channel it allocates the bus to the packet data interface, meantime it delivers the SC delimiter to the bus. Then it uses the first two bytes of the packet to count the packet length and after the end of the current packet transmission it performs one of the following:

1. If there is another packet to be transmitted (up to four) and the packet region still evolves, it delivers another SC delimiter and repeats this procedure.
2. If the current packet is the last to be transmitted, it delivers the EA delimiter.

The Write channel notifies the upper layers for an interrupted packet transmission in order to resume the packet transmission to the successive frames.

IV. EXPERIMENTAL RESULTS

The Access Control Mechanism has been implemented into three double density Eurocards using discrete LSI and MSI integrated circuits (Fast and Advanced Schottky TTL family) because of the required high speed (18 Mbytes/sec) operation. Each board contains a dédicated channel and their intercommunication it achieved through a special interface.

For the experimental purposes, a flexible and versatile pattern generator developed using a 68000 based microproccessor and very fast FIFO buffers. The operational speed of the pattern generator is up to 20 Mwords/sec externally configured.

For the Read channel, the most critical parameter is the required decision time,for the specific delimiter detection,which has to be bounded within a byte period.

The recognition time of the event existence of a frame delimiter in both Read and Sense channels,is 30 nsec. The time required from a specific delimiter recognition is 44 nsec, achieved for a byte clock of about 56 nsec with a duty cycle of 66%. The time to recognize the right of access to the medium depends on the clock's duty cycle and equals to the duration of the positive pulse.

The required time for a packet byte to pass from the interface with the MAU to the interface with the upper layers is 1 μsec for the Read Channel. The respective time for the stream data is 0,5 μsec.

After the notification of the right of access to the Write channel, 38 nsec are required for the first packet byte to appear at the MAU interface, while for the first stream byte 10 nsec are required.

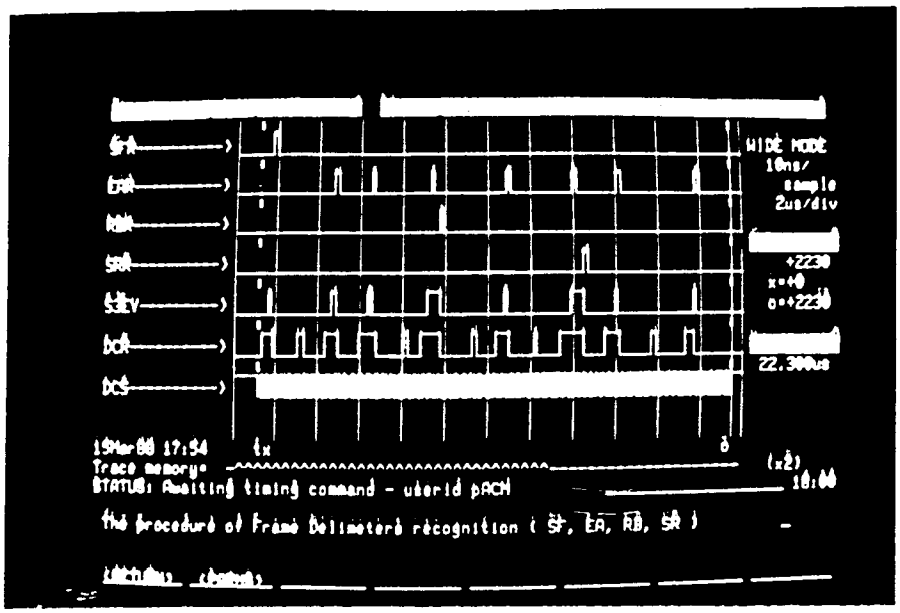

Fig.4. The procedure of Frame Delimiters recognition (SF,EA,RB,SR).

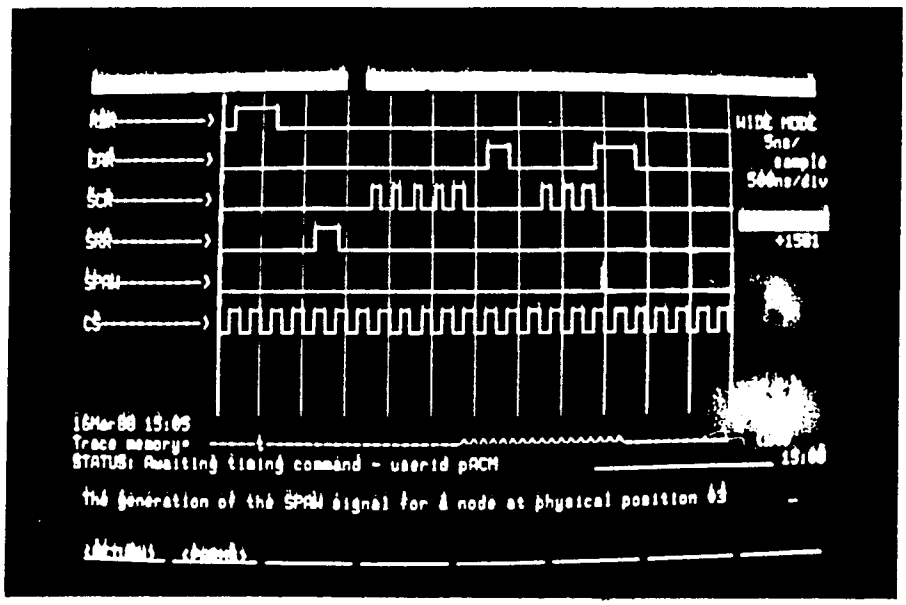

Fig.5. The generation of the SPAW signal for a node at physical position #3.

In Fig. 4, the timing diagram of the procedure of the Frame Delimeters recognition is shown with sampling time of 10 nsec/sample. The timing diagram of the Start of Packet Activity Write (SPAW) signal for a node at physical position #3 is shown in Fig.5.

CONCLUSION

The design and implementation of a high speed access control mechanism for a multiservice LAN with a transmission medium speed of 140 Mb/s is presented.The implementation uses discrete components of the fast TTL family because the operational speed of the system is at 18 Mbytes/s. The observed experimental results show that the required time for a delimiter event recognition of the hybrid frame is 30 ns time which is very well bounded into the byte duration of 56 ns with the duty cycle of 66% and the medium data rate of 144 Mb/s. The control mechanism also provides a continuous monitoring of the down-stream activity of the network providing alarm signals for the abnormal situations to the network management.

The system is totally independent of the structure of the packet and stream data as far as the processing of the communication protocols is concerned and implements in this way the Medium Access Control (MAC) layer functions in absolute conformance with the ISO model for OSI.

Finally, it has to be mentioned that this hardware implementation is of low cost and the architecture of the system is well suited to an advance technology implementation, therefore VLSI custom or semi-custom (e.g. gate array) integrated circuits have to be considered for subsequent prototypes.

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