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Architecture and Implementation of the Access Mechanism for a Bus-Structured Multiservice LAN

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ABSTRACT

The design and implementation of the high speed access mechanism for a fiber optic multiservice LAN is presented. The growing penetration of wideband services in conjuction with a considerable amount of real-time and interactive data traffic requires different handling of stream- and bursty-type communications. This task is accomplished through the use of a distributed hybrid switching protocol which employs an asynchronous dynamic Time Division Multiplexing (TDM) technique. The network comprises a Write channel in which each network node transmits and a Read channel where the transmitted information is duplicated and thus received by the network nodes.In parallel to the Write channel a Sense channel is responsible to detect the right of access for the node.The protocol provides bounded delay for the packet-switched traffic and small buffering memory for the circuit-switched traffic, which together with the network bit rate and the node processing time and capacity set the network efficiency.The experimental results of the implemented access mechanism are presented with respect to the node processing time and the network speed.

I. INTRODUCTION

The effort in the area of the local distribution of data follows, in the last few years, the aspect of integration of many real-time and interactive data services in the same network. The reason for this is threefold [1]:

1) The recent developments in microelectronics and VLSI fabrication, digital signal processing technology, new software technology, optics and optical transmission,may satisfy the most different requirements for the office communications.

2) The "office automation" environment is characterised by a growing penetration of high bandwidth services, like moving video and high resolution graphics beside voice and interactive data.

3) Recent LAN architectures offer very elegant solutions to the local communication problem, basically because of the simplicity in topology and device interconnection and the flexibility in satisfying growth and variability in the environment [2].

The expected workload for such systems will require much higher bandwidth, therefore the use of fiber optics is evident. The optical fibers put,however, some restrictions on the feasible topology because of the reduced power launching efficiency and the unavailability of high impedance taps.The LAN considered in this work is using a unidirectional optical bus based on active tapping where each node is actually a repeater.

The required performance in terms of network efficiency and grade of service offered to each type of traffic in a multiservice LAN has necessitated extensive research activity into hybrid switching systems which enable simultaneous circuit and packet switching, thereby enabling a match of the switching concept to the characteristics of the application [3],[4],[5]. This is because it is well known that circuit switching is more efficient for long messages whereas packet switching is more cost effective for switching short bursty sources of information. The various research efforts based on the packet switching concept as in [2],[6],[7],[8],[9] cannot guarantee the required performance for applications of the stream type other than the voice transmission.

Section II presents the hybrid protocol details and the system description for the access mechanism,in terms of the functions required by the hybrid protocol and its interface with the Medium Attachment Unit which handles the physical layer functions.The overall design and the functional modules of the access mechanism hardware are described in Section III. Finally the experimental behaviour of the system is presented in Section IV.

II. SYSTEM DESCRIPTION

The implemented access control mechanism performs the functions required by the hybrid protocol. The details of the hybrid protocol are presented and then the functional block diagram of the access mechanism in accordance with the protocol.

A. The hybrid protocol

The hybrid scheme of the access protocol for the system under consideration is shown in Fig.1; it is consisting of a hybrid link which is an asynchronous multiplex structure enabling dynamic sharing of the channel bandwidth between the two types of traffic [10],[12]. The circuit-switched calls are prowided with channels characterized by transparency low and almost constant delay, variable capacity without any limitation, very low switching overhead and frame synchronisation. A slot assigned to a circuit-switched communication has a duration proportional to the service bit-rate and it is kept fixed for the entire call duration. The slot position inside the frame varies according to the overall activity evolution thus the synchronism is relaxed allowing a better use of network bandwidth

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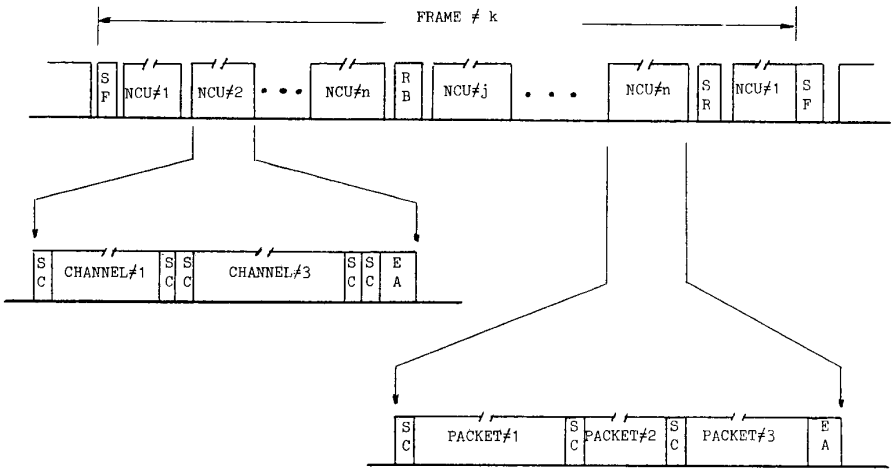

Fig.1. The Hybrid Frame format.

by suppressing the unutilized slots, squeezing the circuit region in real-time and making the spared capacity availlable for packet-switched traffic.The circuit-switched calls are handled on a loss basis whereas packet-switched calls are served on a delay basis. Finally signalling related to circuit-switched communications is packet-switched.

The activity on the digital channel is organised in contiguous periodic frames of a duration of 5 ms. Each frame is constituted by two regions the circuit and the packet. The beginning of a frame is marked by a Start-of-Frame (SF) delimeter.The beginning of the packet region is recognized by the Region-Boundary (RB) delimeter. Every frame includes only one circuit round whereas may include a variable (integer or not) number of packet rounds, as a consequence an explicit Start-of-packet-Round (SR) delimeter is used. If a packet round cannot be completed during a single frame it must be resumed in the successive frames starting at the exact point where it was interrupted.

The network nodes are numbered in accordance with their physical position on the bus and each node knows the maximum number N of the nodes, and it access the bus in an ordered sequence, like in the Round Robin TDMA algorithm. In the circuit region, when a node has the access right,each circuit communication begins with the Start-of-Channel(SC) delimeter. If a channel has nothing to transmit it just sends the SC delimeter. Each node denotes the end of its access activity by the End-of-Activity (EA) delimeter. In the packet region the nodes follow the same procedure and each node in a packet round transmits a maximum of three packets.The length of the packet varies from a minimum of 256 bytes to a maximum of 4 Kbytes. In the beginning of each packet it is the SC delimeter and at the end of a node activity the EA delimeter.In both regions if a node has nothing to transmit does not perform any operation and the next higher in order node after a Time Out time(TL) gets the bus.The most upstream node is responsible to generate the frame delimeters but all the nodes are capable to do it providing a fully distributed management of the frame.

B. The Access Control Mechanism

The network nodes communicate with the physical interface mechanism the Medium Access Unit (MAU) through a Write channel and a Read channel.Each node transmits to the Write channel and receives from the Read channel; all the information of the Write channel is heard by all nodes through the Read channel. Moreover each node can follow the upstream activity on the Sense channel which is placed in parallel with the Write channel. The same configuration is implemented by the MAU.

The MAU carries out the typical transmission tasks like signal regeneration, timing extraction bit alignment,coding-decoding and the electro-optic interface to allow the exchange of user and control information between the network nodes [12]. The CMI code is used because it leads to an easy and reliable implementation of the hybrid protocol delimeters through the use of code violations. The CMI is coding the "1" by level 1 or 0 alternatively on the entire bit period and 0 on the next one; the "0" is coded by a 0 level on the first half of the bit period, and 1 on the second. The delimeters SF,EA,RB,SR are repeated three times for redundancy and their detection is based on a majority rule; the SC does not follow this redundancy because a transmission error does not affect the functionality of the protocol.

The interface of the MAU to the access mechanism is implemented in a parallel form. After the serial to parallel conversion the interface distinguishes data and delimeter bytes by means of proper signals. The interface includes:

1. To the Read channel of the access mechanism an 8-bit data-command bus, clock and control signals to distinguish between data and commands and an indication if a coding error has been detected for each transfered byte.
2. To the Sense channel a 4-bit command bus,the clock and the indication for a coding error for each transfered command.
3. From the Write channel an 8-bit data-command bus and strobe signals. The Write channel accepts an indication from the MAU for the required bit-stuffing periods.

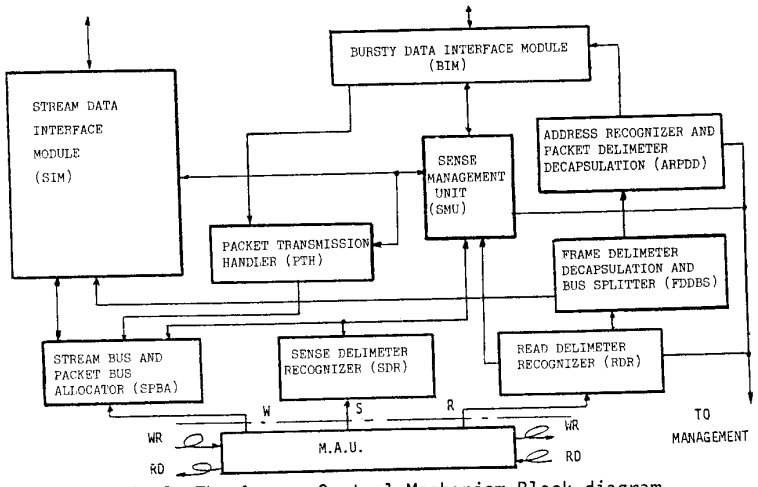

Fig.2. The Access Control Mechanism Block diagram

Fig.2 shows the functional blocks of the access control mechanism. The three blocks perform the following functions.

The Sense block is responsible during the entire operation of the hybrid protocol to recognize the frame delimeters in order to keep count of the activity of each network node.During the frame time the Sense Management Unit (SMU) taking indications from the Sense Delimeter Recognizer (SDR) determines the evolution of the hybrid protocol. In the case of normal evolution of the hybrid frame the SMU recognizes the right of access for the node and notifies the Write block to begin activity.The SMU has also the timers for the counting of the TL time for a node that has nothing to transmit. It also notifies the Write block if there are no data for the circuit or the packet region to transmit the required protocol delimeters as they are described in Section II. Finally the SMU is responsible for the allocation of the Write bus to the Stream data Interface Module (SIM) which is responsible for further processing of the Stream data, or to the Packet Transmission Handler (PTH). In the case of abnormal evolution of the hybrid frame the SMU notifies it to the node manager for further proccessing.

The Write block works in conjuction with the Sense block. When the SMU notifies the STH during the circuit region to pass transparently the stream data from the stream data buffer to the Stream and Packet Bus Allocator (SPBA). During the packet region the SMU notifies the PTH which adds to the packet data the required SC and EA delimeters at the beginning of each packet and at the end of the packet region transmission respectively and on the same time the SPBA to allocate the bus to the PTH. The SPBA detects the bit-stuffing signal from the MAU and is responsible to relax the Write block activity for the bit-stuffing time.

The Read block is totally independent from the two other blocks. It recognizes the normal frame evolution through the Read Delimeter Recognizer (RDR) and then the Frame Delimeter Decapsulation and Bus Splitter (FDDBS) is responsible to distinguish the received data to stream and packet.Then after the frame delimeters decapsulation the stream data are delivered to the SIM and the packet data if they are intented for the current node are delivered to the Bursty data Interface Module (PIM) which is responsible for further processing of the Packet data after the SC delimeter decapsulation through the Address Recognizer and Packet Delimeter Decapsulation (ARBBD). Finally the Read block notifies the management of the node when it detects abnormal evolution of the frame delimeters.

III. SYSTEM IMPLEMENTATION

The MAU and the access control mechanism have been implemented on five boards. The electro-optic interface and the MAU are implemented using printed circuit techniques. The access mechanism involves three VME high density boards and it is implemented using wire-wrap techniques.

The electro-optic interface characteristics are:

i) Laser source with automatic control
ii) PIN detector
iii) Transimpedance input amplifier for the receiver with sensitivity better than -38 dbm at 10-9 BER with a dynamic range of 20 dB. The MAU implementation uses Emmiter-Coupled-Logic (ECL) discrete components at a clock rate of 140 Mb/s.

The access control mechanism receives data at a speed of 17.5 Mbytes/s. The high speed of operation imposes the use of discrete LSI and MSI components of the fast TTL family.

Fig.3 the shows hardware modules of the Read block. The RDR module of Fig.2 has a complicated task to perform because the SF,RB,SR,EA delimeters are structured as 3-bytes for redundancy purposes. Therefore the RDR module has to search on "windows" of four concecutive bytes to recognize a frame delimeter event (repeated three times) and then to follow a majority rule which requires a delimeter code to be detected at least twice inside the four byte pattern in order to have a specific frame delimeter recognized. There exist four possible structures for the "window" ; denoting by S_3 the code for a 3-byte delimeter,S_1 the SC,E a data or command byte with a coding error,D a data byte, and X a generic data, signal or error word we obtain:

1) Detection of three contiguous S_3 bytes

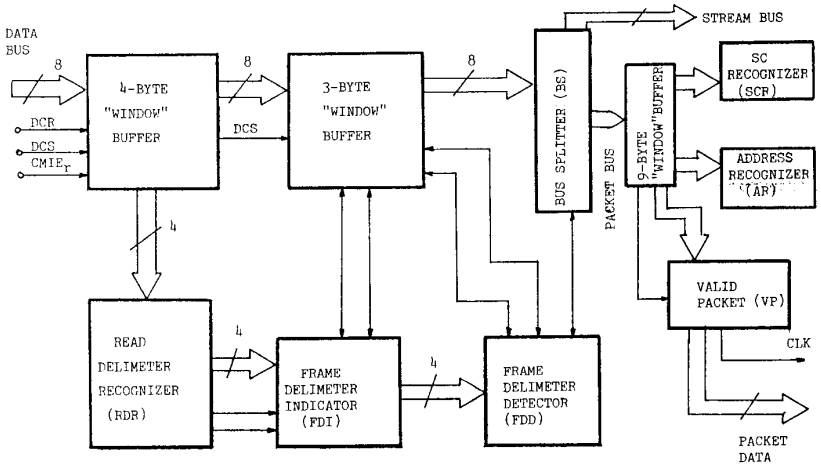

Fig.3. The Read Channel Block Diagram.

2) Detection of two contiguous S_3 bytes
3) Detection of two non contiguous S_3 bytes
4) Detection of one S_3 byte

The Frame Delimeter Indicator (FDI) of Fig.2 using either the first three or the last three bytes of the "window" notifies the existance of a S_3 delimeter. The various possible decisions are summarized in Table I.Following the Frame Delimeter Detector (FDD) through the use of a 3-byte "window" (majority rule) detects the frame specific delimeter. Then the Bus Splitter discriminates the stream and the packet data. The packet data are processed,for the current node address matching and the SC delimeter decapsulation through another 9-byte "window" because of the packet structure which is the following:

i) The first byte is the SC delimeter
ii) The second and the third bytes indicate the packet length
iii) The fourth to the ninth bytes are the node address.

Then the packet is delivered to the BIM while the stream data are already delivered to the SIM.

Fig.4 shows the hardware modules of the Sense block.This block has the same structure as the Read block up to the point where the specific delimeter is recognized with the exeption of a 4-byte bus used because it accepts only command bytes from the MAU. The procedure of the delimeter detection is similar to the one described for the Read block and it is carried out through the Sense Delimeter Recognizer (SDR) and the FDI and FDD modules of the Sense block. The Alarm Generator (AG) in conjuction with the FDD is generating the alarm signals in the case of abnormal hybrid frame delimeters evolution, which are directed to the node manager. It also provides to the node management the node statistics in conjuction with the Read block FDD module. The Time-Out Timer (TLT) is counting the evolution of a network node which has nothing to transmit and in conjuction with the Physical Address Recognizer (PAR) are responsible for the generation of the stream and packet region start of activity signals (SSAW,SPAW respectively) for the current node that are directed to the local Write block. Finally the FDD denotes to the Write block the end of the

TABLE I: Decoding Rules for the Frame Delimeters

Possible "window" structures	4-byte "window"	3-byte decision "window"	Decision
A	$S_3\ S_3\ S_3\ X$	$S_3\ S_3\ S_3$	S_3
B	$S_3\ X\ S_3\ X$	$S_3\ X\ S_3$	S_3
C_1	E S_3 S_3 E	- - -	Alarm
C_2	E S_3 S_3 S_1	E S_3 S_3	S_3
C_3	E S_3 S_3 D	E S_3 S_3	S_3
C_4	S_1 S_3 S_3 E	- - -	Alarm
C_5	S_1 S_3 S_3 S_1	S_1 S_3 S_3	S_3
C_6	S_1 S_3 S_3 D	S_1 S_3 S_3	S_3
C_7	D S_3 S_3 E	S_3 S_3 E	S_3
C_8	D S_3 S_3 S_1	S_3 S_3 S_1	S_3
C_9	D S_3 S_3 D	- - -	Alarm
D	X X S_3 X	- - -	Alarm

A: Three S_3 contiguous signals detected
B: Two not contiguous S_3 signals detected
C: Two contiguous S_3 signals detected
D: One S_3 signal detected

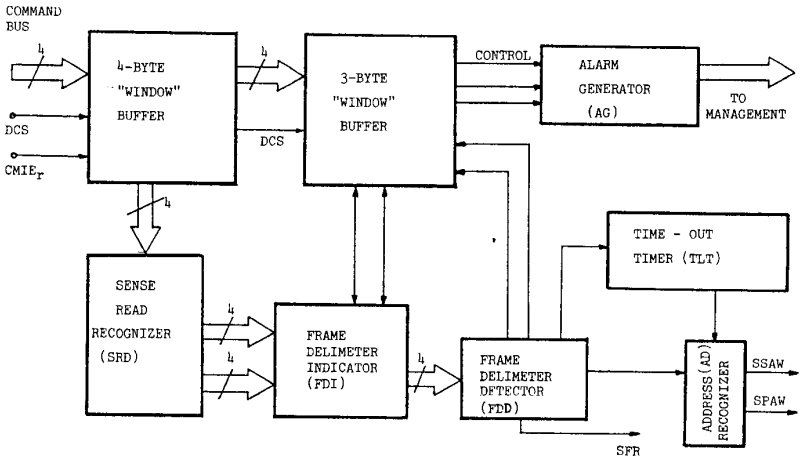

Fig.4. The Sense Channel Block diagram.

packet region (SFR signal) in order to stop transmission of packet data.

In Fig.5 the hardware modules of the Write block are shown. When the Sense block detects the right of access for the current network node in the circuit region the Bus Allocator (BA) directs the data bus to the SIM which transparently passes stream data that already include the required protocol delimeters (SC,EA). In the meantime the Data-Command Strobe Multiplexer (DCMx) in conjuction with the Local and Tx Clocks Generator (LTxCG) notifies the MAU for a transmit session and delivers the required strobe signals for the data and command bytes. When the Sense block detects the right of access in the packet region the Delimeter Generator (DG) delivers the SC delimeter at the data bus which now is allocated to the Packet Data Bus (PDB) through the BA. Then the Packet Length Tx Counter (PLTxC) counts the length of the packet and after the end of the current packet transmission it performs one of the following:

1) If the Round Evolution Counter (REC) indicates that there is another packet to be transmitted and the packet region still evolves, notifies the DG to deliver another SC byte, then repeats the same procedure.

2) If the REC indicates that the current packet was the last to be transmitted, it triggers the DG to deliver an EA byte (repeated three times) to the Packet Bus Multiplexer (PBMx).

The PBMx is responsible to multiplex the command and data bytes for the PDB according to the protocol rules.The LTxCG receives the bit-stuffing indication signal from the MAU and controls the DCMx and PBMx modules for the required relaxation time through an internal timer for the bit stuffing period. During the transmission of packet data the reception by the REC of the Start-of-Frame delimeter Recognized (SFR) signal from the Sense block stops the transmission and a signal is generated that stops the PLTxC in order the transmission to be resumed at the next frame.

The interface of the access control mechanism to the upper layers is realized through two interface boards, under implementation, which include two separate FIFO buffers,one for receiving and one for

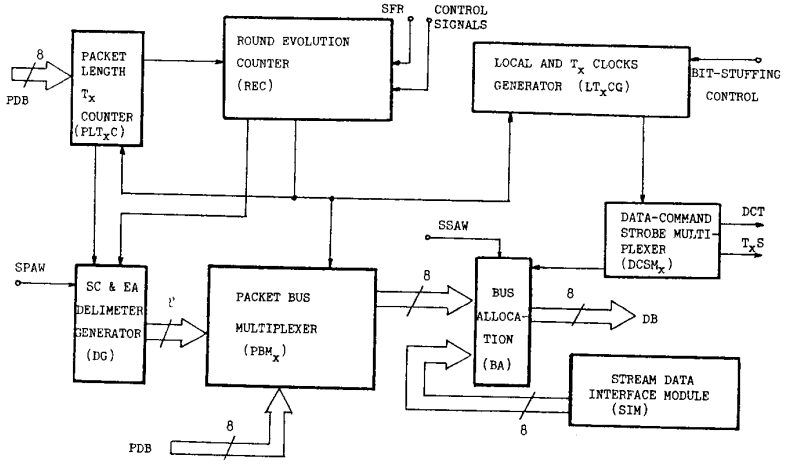

Fig.5. The Read Channel Block diagram.

transmitting, and the FCS generation-checking mechanism.The transfers from/to the interface boards are controlled by the access control mechanism and they are asynchronous.

The experimental performance of the system is summarized as follows:

1) The response time of the Sense and Read blocks for the recognition of the event S_3 frame delimeter is 30ns.
2) The response time of the Sense and Read blocks for the recognition of a specific delimeter is 44ns for a byte clock with a duty cycle of 66% which is also the time required from the access mechanism to recognize the right of access to the medium.
3) The Read block requires for the first packet byte from the interface with the MAU to the interface with the packet buffers 1 μs and for the first stream byte 0.5 μs.
4) The time required for the Write block after notification of the right of access for the first packet byte to appear at the MAU interface is 38 ns and for the first stream byte is 10 ns.

CONCLUSION

The design and implementation of a high speed access control mechanism for a multiservice LAN with a transmission medium speed of 140 Mb/s is presented. The implementation uses discrete components of the fast TTL family because the operational speed of the system is at 17.5 Mbytes/s. The observed experimental results show that the required time for a delimeter event recognition of the hybrid frame is 30 ns time which is very well bounded into the byte duration of 56 ns with the duty cycle of 66% and the medium data rate of 140 Mbs. The control mechanism also provides a continuous monitoring of the down-stream activity of the network providing alarm signals for the abnormal situations to the network management.

The system is totally independent of the strucuture of the packet and stream data as far as the processing of the communication protocols is concerned and implements in this way the Medium Access Control (MAC) layer functions in absolute conformance with the ISO model for OSI.

Finally it has to be mentioned that this hardware implementation is of low cost and the architecture of the system is well suited to an advance technology implementation, therefore VLSI custom or semicustom (e.g. gate array) integrated circuits have to be considered for subsequent prototypes.

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