Architecture and implementation of an adaptive nanopositioning controller for fast spiral scanning

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***Abstract*—Nanopositioning is a key factor for a wide range of applications, such as surface imaging and ultra-high-density probe-based data storage. These applications use scanning probes in order to sense and alter the properties of the underlying medium with nanoscale precision. Recently, new scanning schemes were introduced that can lead to high-speed nanopositioning, if their inherent properties are properly exploited by the tracking control mechanism. The aim for high-speed operation poses stringent requirements to the controller architecture, in terms of speed of execution and arithmetic accuracy. In this paper we present the design of a linear time-varying controller for high-speed, constant linear velocity archimedean spiral scanning. This effort includes the design and implementation of such a control scheme, as well as a flexible multi-board hardware and software test-bed for nanopositioning systems. For proof of concept, the presented controller is applied to an experimental AFM-based scanning probe setup in order to track spiral trajectories efficiently.**

***Index Terms*—Archimedean spiral, nanopositioning, control, DSP, FPGA.**

I. Introduction

Fast and ultra-precise positioning is of major significance for rapidly emerging applications that use scanning probe techniques in order to observe, manipulate and alter materials down to the nanometer scale [1], [2], [3]. In such a system, nanopositioning scanners with 2-D motion capabilities are used to displace a sample laterally and longitudinally, relative to a probe equipped with a nanometer-sharp tip [4].

One way to achieve high-speed operation is to use the recently introduced spiral nanopositioning scheme, where motion starts from an initial point of radius r_{min} from the sample center and follows a spiral trajectory of equidistant turnings around the center of the medium's x/y-plane, until a maximum radius r_{max} is reached. This type of spiral positioning results in a narrowband reference position signal of variable frequency, which can be exploited by the control architecture in order to enable high-speed operation. An in depth analysis of the spiral scheme and the control architecture under consideration is presented in [5], [6], [7], [8] and in the references therein.

The aim for high-speed operation poses stringent requirements to the controller architecture and implementation. Furthermore, in order to test the controller in real conditions, a test-bed is necessary, with which one is able to efficiently implement and flexibly integrate the controller with the overall mechanical system. In this paper we present the design of a linear time-varying controller that achieves precise high-speed constant linear velocity when used in tracking of an archimedean spiral trajectory. For proof of concept, the presented controller is applied to an experimental Atomic Force Microscopy (AFM) scanning probe setup, in order to evaluate the controller on tracking of fast spiral trajectories. An overview of the nanopositiong system is depicted in Fig.1.

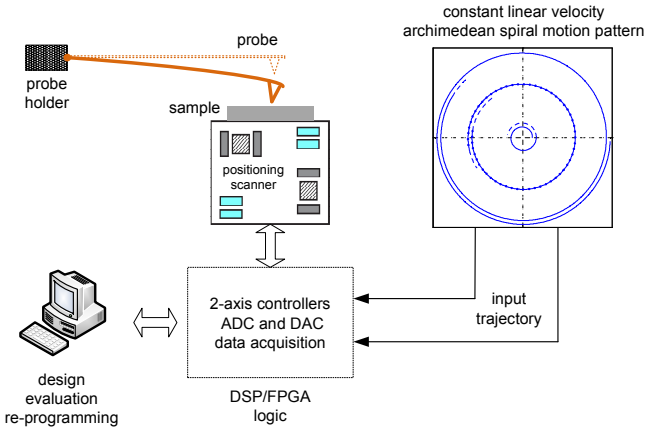

Fig. 1. Overview of spiral nanopositioning.

The rest of this paper is organized as follows: Section II describes the experimental AFM-based setup, while Section III presents in brief the considered control architecture and the control design process and the implementation of the proposed controller. Finally, Section IV highlights the controller's test and evaluation process along with its integration into the experimental setup.

II. Experimental setup

The nanopositioning system under consideration is depicted in Fig.2. It is based on a piezoelectrically actuated scanner, capable of displacing the sample (thin polymer film) with respect to the cantilever tip in the x and y axis. The travel ranges are 100 μm for both axes. Position information in the x/y plane is provided by two high-precision capacitive sensors, one for each direction of motion.

The cantilever lying in a fixed position above the moving sample has thermomechanical read and write capabilities,

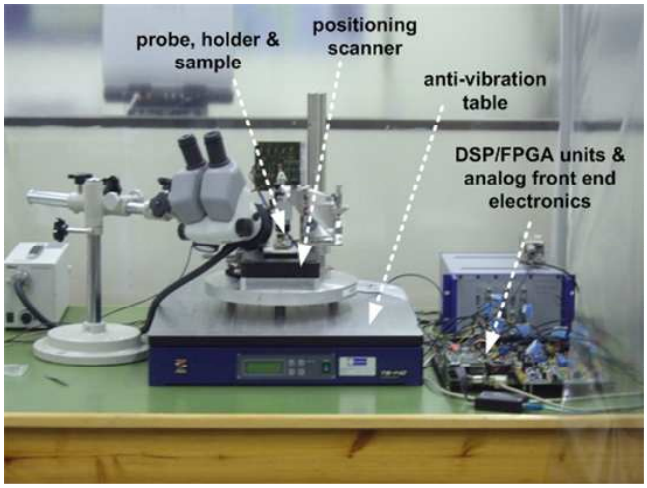

Fig. 2. AFM-based scanning probe experimental setup.

although other sensing methods (like laser deflection) can also be used. When used as a probe storage system, information is stored as sequences of indentations on the thin polymer film. Thermomechanical writing is performed by applying an electrostatic force to the polymer layer and simultaneously softening the polymer layer by local heating. Readback is achieved by measuring the local thermal conductance between the probe and the sample. The presence or the absence of indentations corresponds to logical 1s or 0s, respectively. The entire mechanical system lies on an anti-vibration table to prevent the system from environmental shocks and vibrations, which can seriously affect the positioning accuracy and the system's overall performance.

A custom base-board provides all the necessary circuitry for driving the mechanical system with the appropriate control analog signals and for acquiring the sensor feedback signals [1]. Moreover, the base-board hosts the digital signal processing (DSP) and field-programmable gate array (FPGA) boards used for control implementation, data acquisition and host communication.

III. Nanopositioning Controller Architecture

In each axis, the constant linear velocity archimedean spiral reference signal is a very narrowband frequency-shifting signal with varying magnitude. Moreover, the way that both the center frequency and the frequency range of the signal depend on the instant spiral radius for a given constant linear velocity is known a priori and is appropriately exploited by the controller for increased spiral tracking efficiency.

Two individual controllers with identical architecture are used for the control of the nanopositioner, one for each axis of motion. Figure 3 shows the block diagram of the controller and presents in brief the system identification and design process of the loop's components. Note that only the x-axis case is depicted here, but the results hold as is for the y-axis case. The first order loop comprises a frequency-sliding peak filter, an H_∞ controller denoted by H_∞, and a notch filter denoted by K_{NF}, all connected in a cascade manner. For the design of the time-invariant part of the controller, the H_∞ control design was used. The sixth-order transfer function fits of the experimentally identified scanner system used during the controller synthesis produced eighth-order H_∞ controllers in both axes.

The shape of the time-varying peak filter can be seen in Fig.3. The filter's center frequency shifts continuously in time, adjusting to the corresponding shift of the center scan frequency along the spiral trajectory. Its value at the time instants of interest can be calculated in advance as a function of the spiral radius along the trajectory. The filter parameters M, N, Δ are selected according to the desired magnitude response of the filter, and are illustrated qualitatively in Fig.3. Specifically, M denotes the magnitude in dB at the instantaneous center frequency, and N the magnitude in dB at the frequency points around that frequency, which are determined by the value of the variation Δ. For a more thorough analysis on peak filters see for example [9].

Finally, in order to compensate for any residual unmodeled resonances, a notch filter denoted by K_{NF} is used. The resulting overall x-axis sensitivity transfer function, relating the reference input with the tracking error signal, and complementary sensitivity transfer function, relating the reference with the output, are depicted in Fig.3 (in fact, snapshots of the transfer functions when the peak filter acts at around 20 Hz). Note that an in depth analysis of the loop design process can be found in [6] for a similar scanner system.

The cascaded controller structure of Fig.3 was implemented on a 300 MHz TMS320C6713 floating-point digital signal processor (DSP) from Texas Instruments (TI). Although this is not the most efficient option in terms of execution time, a DSP implementation offered a rather good trade off between implementation flexibility/complexity and performance. Besides that, the key aim of this work was not a fully optimized controller implementation, but a flexible hardware and software framework for the fast prototyping and test environment of such an architecture, that yet meets the performance requirements imposed by high-speed nanopositioning operations.

Based on the architecture described in Section III, an overall 12-th order controller was realized, resulting from the individual components of the loop, namely the 8-th order H_∞, the 2-nd order notch and the varying-coefficient 2-nd order peak filters. The realization was in direct-II second order sections (biquad).

IV. Evaluation and Experimental results

In order to provide a flexible framework for integration, test and evaluation of the developed controller, a complete test-bed was developed using a multi-board environment that comprises of two daughter boards, each of which holds a 300 MHz TMS320C6713 floating-point DSP and a Xilinx Virtex II FPGA. Both daughter boards are hosted on the base motherboard described in Section II in a packed configuration, enabling the passing of a large number of signals used for

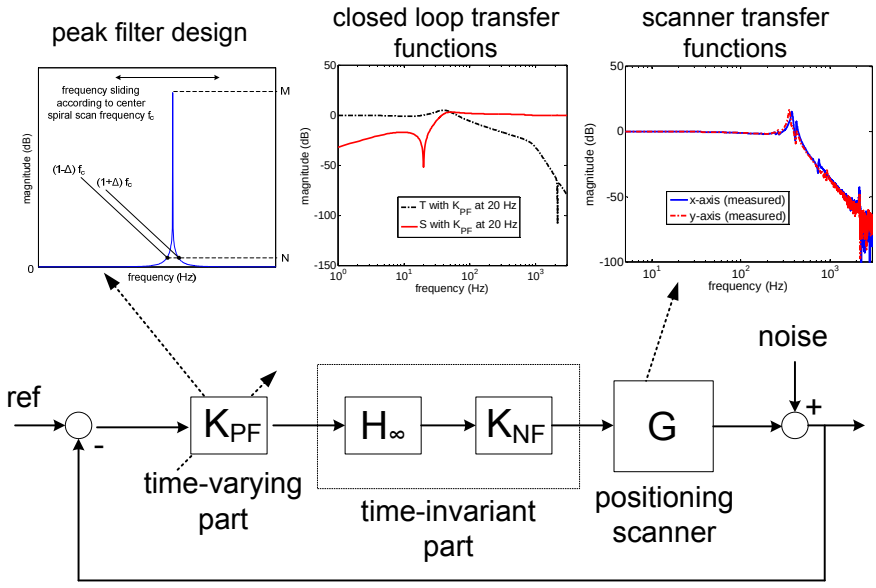

Fig. 3. Nanopositioning control architecture and design overview.

custom inter-board communication. The spatial arrangement of the two daughter boards and the motherboard is illustrated in Fig.4. It has to be mentioned, that this is the currently used prototype for surface imaging, designed a few years ago, and a new prototype is under development that is based on more advanced V6 FPGAs and a multicore DSP engine with an 8-core C6678 floating-point processor, each of which runs at 1.25 GHz, and high-rate serial I/O integrated peripherals.

The functional description of the overall system and testbed is shown in Fig.5. The top layer daughter board (Data Acquisition and Interface Board) implements the data-acquisition modules that provide finite state machines (FSM), for synchronously collecting a large number of signal data, including ADC/DAC values, cantilever readings and control signals. On the DSP side, the FireWire protocol stack is implemented. The FireWire interface is used for the communication between the daughter board and the host. That includes transfer of system configuration parameters and the collected data back to the Matlab environment for evaluation and performance analysis.

The main task of the bottom layer daughter board (Control Board) is the implementation of the prospective controllers. This is done on the DSP, while FPGA logic implements a shadow lite version of the data-acquisition engine described earlier responsible for clocking the data to be collected to be transferred to the top layer board. The system configuration parameters are passed from the Interface Board to the Control Board before the data-acquisition modules are initiated. For parameter transfers, a dual-port RAM is used as shown in Fig. 5. Moreover, a host PC running Mathworks' Matlab/Simulink environment and TI's Code Composer Studio (CCS) integrated development environment was used for the design of the controllers, the (re)programming of the DSPs and the configuration of the overall system's parameters via a custom Graphical User Interface (GUI). The resulting configuration can be used

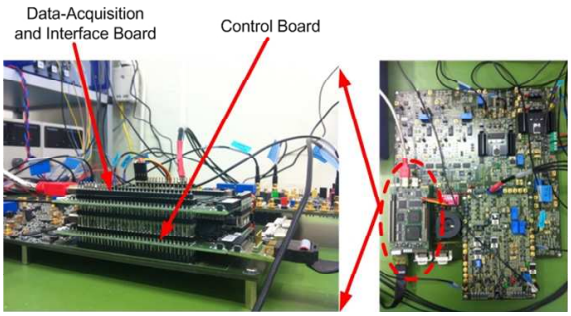

Fig. 4. Multi-DSP/FPGA controller test-bed.

as a versatile and fully parameterizable integration, test and control environment for a wide range of nanopositioning and scanning probe systems.

Using a floating-point (FP) DSP engine for executing the control algorithms is a flexible and user friendly approach but it has various limitations as the sampling rate increases. Execution of a control algorithm in a DSP engine is based on three distinct phases. At the initial phase the incoming data (ADC and reference values) are retrieved, then the control loop is executed and at the final step, the new DAC values are provided to the system under control. In some cases overlapping of the initial and the final phases can be performed. The execution time of the two data transfer phases is independent to the complexity of the control algorithm and is determined by the used I/O technology. When high speed links are used for transferring the ADC/DAC values the transfer time is minimized, but an additional protocol overhead is introduced and the hardware complexity increases. As the sampling rate increases, the total execution time for the control algorithm decreases, and hence, the available time for the control loop decreases drastically.

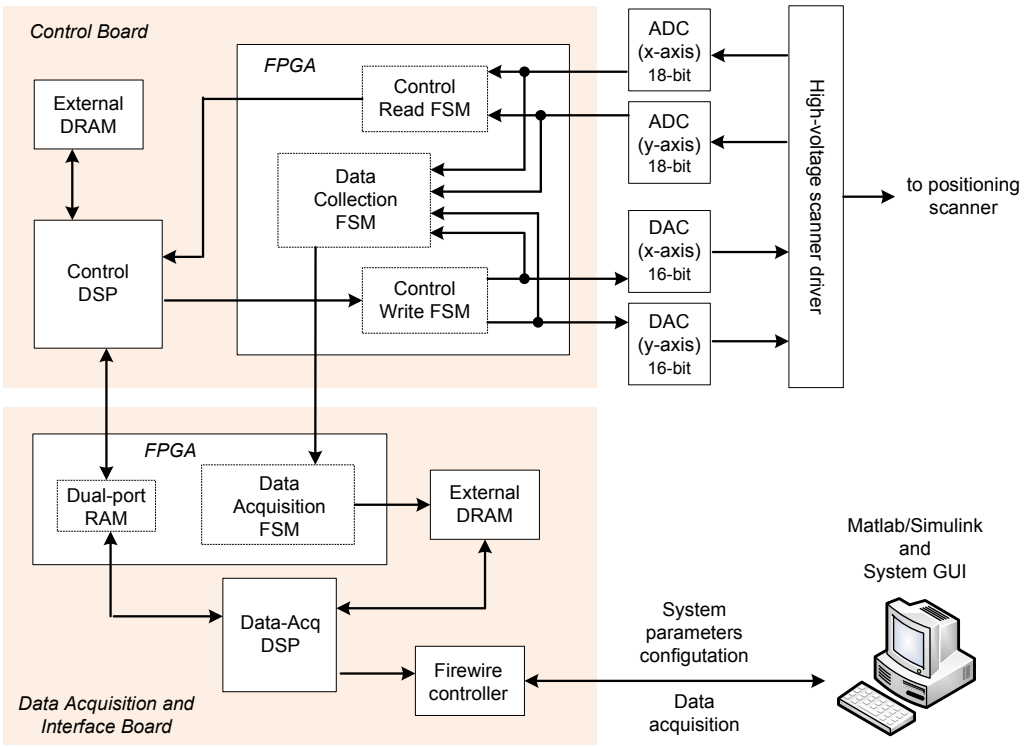

Fig. 5. Overview of hardware and software prototyping platform.

One approach for solving that problem is to increase the DSP clock speed or to use a DSP engine with multiple cores. Another approach for implementing the floating-point control algorithms at high speed is by using custom floating point modules which will be directly attached to the ADC/DAC units. FPGA vendors (e.g. Xilinx Floating-Point Operator IP [10]) provide some basic building blocks for that case but the DSP flexibility is lost. For example, when a DSP core is used, the modification of the control loop during system debugging is performed by re-compiling the source code and downloading the new code to the DSP engine, while using the FP FPGA approach, this procedure requires resynthesizing and rerouting at least part of the FPGA, a time consuming procedure. The same also holds for data acquisition and analysis during the control loop evaluation process.

As a next step in our work, we plan to organize the prototype using a hybrid approach. The prototype will have the capability to communicate with a high-performance floating-point DSP engine using a Gbps serial link, and also the required FPGA glue logic for implementing the final control algorithm in hardware. As a first step the control algorithm will be implemented in the DSP, probably executed at a lower sampling rate, and when the evaluation process will be completed, the same algorithm will be implemented in custom hardware.

V. Conclusions

In this paper the design and prototyping of a type of tracking controllers for spiral nanopositioning was presented. Apart from the design and the DSP implementation of the nanopositioning controller, a versatile and fully configurable test-bed was presented. In its current configuration, the test-bed enables efficient testing of a variety of prospective controllers and data acquisition for signal analysis during testing and debugging.

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