A Versatile Platform for Characterization of Solid-State Memory Channels

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***Abstract*— This paper presents a versatile hardware platform designed for high performance characterization and testing of non-volatile memories. The platform is based on a reconfigurable hardware-software architecture with high degree of multi-domain testing and data acquisition capabilities. The platform constitutes a valuable tool for statistical characterization of the solid-state memory channel for new and emerging non-volatile memories with the goal to study the noise and interference sources that affect the reliability of these devices. We describe the architecture of the hardware testbed and demonstrate its functionality with experimental results from phase-change memory and flash memory devices.**

I. Introduction

Over the past few years, non-volatile memory (NVM) has emerged as possible replacement for main memory and hard disk drives (HDDs) [1], [2]. In addition, new memory technologies are examined for their potential to provide cost- and power-effective solutions for exascale systems [3]. New generation NAND Flash memory offers increased read/write bandwidth and memory capacity achieved by advances in cell design, array architecture and multilevel cell (MLC) operation [4]. Phase-change memory (PCM) belongs to the broader class of resistive non-volatile memories that are often described as universal, i.e., spanning characteristics of both storage as well as memory devices [5]. In addition, PCM offers multi-bit operation which is essential for increasing the capacity and reducing the cost per bit. At the same time other memory technologies, such as Resistive RAM (RRAM) or Spin-Torque Transfer MRAM (STT-MRAM) are explored based on their unique advantages as candidates to replace incumbent memories [6].

As the memory industry moves to smaller fabrication nodes, MLC technology becomes even more difficult to achieve. The read noise becomes severe while cell-to-cell interference (CCI) starts to play an important role in the reliability of the read-back signals. With technology scaling, CCI is expected to be a dominant interference source in MLC Flash memory [7]. In PCM, resistance drift is a unique phenomenon that appears immediately after programming and affects the reliability of detecting multilevel stored information [8]. Apart from the advances in the process, array and circuit front, the adoption of advanced signal processing and coding techniques is considered essential for enabling MLC technology in emerging NVMs [9]–[11].

Proper understanding of the noise characteristics of the memory channel is crucial in order to assess the capacity of the channel as well as for the design of signal processing and coding schemes tailored to characteristics of these devices. In this paper we present a versatile hardware platform designed for high performance characterization and testing of non-volatile memories. The platform is based on a reconfigurable hardware/software architecture with high degree of multi-domain testing and data-acquisition capabilities. It provides a valuable tool for statistical characterization of the solid-state memory channel for new and emerging non-volatile memories. We describe the architecture of the hardware platform and demonstrate its functionality with experimental results from PCM and NAND Flash memory devices.

II. Versatile Hardware Testbed

The design goal of the non-volatile memory testbed was to build a high performance data acquisition and characterization platform for non-volatile memories, which at the same time will allow the implementation and testing of various signal processing algorithms and circuits in order to evaluate their performance on the device under test, especially for MLC non-volatile memory technologies. Fig. 1 shows a block diagram of the general architecture of the platform, which consists of three main units:

- a high-performance analog-front-end (AFE) board that contains a number of digital-to-analog and analog-to-digital converters (DACs and ADCs) along with discrete electronics such as power supplies, voltage and current reference sources, voltage translators, etc.,
- a FPGA board that implements the data acquisition and the digital logic to interface with the memory device under test and with all the electronics of the AFE board, and
- a second FPGA board with an embedded processor and Ethernet connection that implements the overall system control and data management as well as the interface with the data processing unit.

Embedded microcode allows the execution of experiments ranging from single cell characterization up to full device characterization for endurance and retention purposes. These experiments may comprise generation of synchronized patterns, either as single shot or in repetitive mode, sensing of signals using multiple rates and internal feed-back functions that may alter the experiment execution on-the-fly, depending on real-time extracted parameters. The use of dedicated FIFOs per HW module along with a multi-thread microcode for

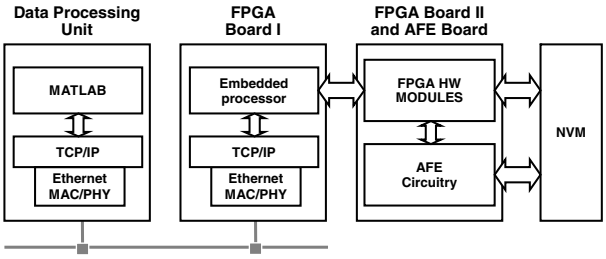

Fig. 1. Overall description of NVM testbed.

FIFOs handling and a modular host software architecture enables the execution of experiments with a few GBytes data acquisition capability which facilitates the characterization of the NVM devices in terms of bit-error rate (BER), write time, location of errors, etc.

A. Modular Hardware Architecture

The NVM testbed was built around a modular hardware architecture that enables the simultaneous utilization of the AFE electronics along with HW and SW modules that implement standard or custom algorithms for memory-related functions and testing. Fig. 2 describes the overall architecture of the NVM testbed. The system controller is implemented in an embedded processor running a Linux kernel and the program code is organized in various threads that coordinate the communication with the data processing unit and the management of the various hardware and software components for executing multiple commands in different sets of hardware modules. The interface with the data processing unit is based on the TCP/IP protocol stack and uses a seamless data transfer protocol that is described in the next subsection. The AFE circuits as well as the memory device under test are interfaced using dedicated HW modules. Each HW module contains a set of control and status registers along with a set of data-in and data-out FIFOs of programmable size that serve for storing the samples of input analog waveforms or of digital output pattern generators.

A number of function-specific HW modules have been implemented in the testbed. These are stand-alone modules which communicate with the system controller using a common peripheral interface for management purposes and use a dedicated interface for synchronization purposes. Each module implements a specific function, either in the digital or the analog domain. Multiple modules of the same type are used concurrently to support a large number and variety of experiments. A few examples are given next:

- a HW module implements the interface with an external ADC, i.e., it provides the digital signals and the programmable sampling clock to the chip and stores the ADC values to an internal FIFO,
- a HW module implements the interface with an external DAC, i.e., it provides the digital output pattern and the trigger clock to the DAC, while the output data pattern is retrieved from a pre-stored FIFO which may be scanned ones, repetitively or in sync with another HW module,

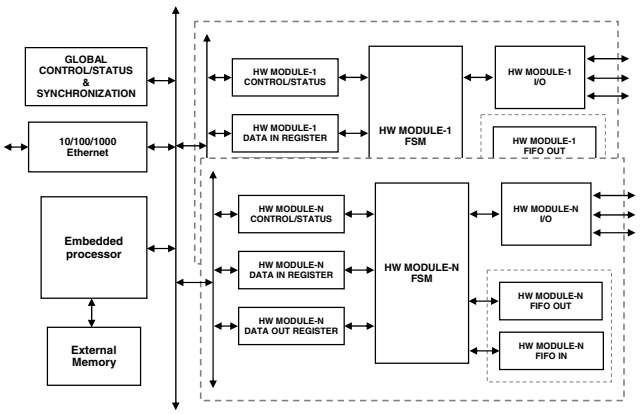

Fig. 2. Block diagram of the overall NVM testbed HW architecture.

- a HW module implements an arbitrary pulse pattern waveform, i.e., on-off events required by external components using a number of digital output signals,
- a HW module implements the interface with the memory device under test, i.e., the addressing interface, the programming-mode or read-mode interfaces, etc.

In the heart of each HW module is a finite-state-machine (FSM) which is triggered and monitored by the system controller via dedicated control and status registers. Attached to the FSM is an output-data FIFO and/or an input-data FIFO which are used to store the sequence of output events and the incoming data from the external devices respectively. The notion of output events includes, for example, the sequence of digital values that modulate the DAC output at a given rate. The incoming data are measurement data coming either by measurements units, such as ADCs, or directly interfacing the memory under test. Downloading the sequence of events to a HW module's output FIFO or uploading the series of measured samples from a HW module's input FIFO is implemented at the system controller by using dedicated DMA engines, which store/retrieve the data from the main memory of the system. The main memory is used as a temporary buffer between the various hardware modules and the data processing unit. Data mirroring is achieved by using a specific TCP/IP based application.

For the synchronization of the various hardware modules during testing, a dedicated microprocessor-controlled HW module is used that implements the global control and synchronization of the different stand-alone modules. The goal of the synchronization unit is to activate/deactivate circuits on different HW modules and to implement iterative testing sequences. This is achieved by using a programmable FSM that senses the status of the various hardware modules and based-on a set of experiment-specific commands it sets the proper control signals.

B. Data Transfer Protocol

The interface between the HW testbed and the data processing unit, i.e., the host computer, is based on the TCP/IP protocol stack and a seamless data transfer protocol. The latter

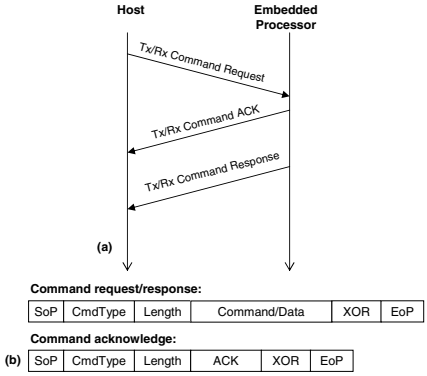

Fig. 3. Data transfer protocol between the HW platform and the host.

allows the user to have direct access to the system controller's main memory as well as to the individual HW modules memory space, and therefore to the various electronics of the testbed. This approach allows the user to run different testing scenarios and to collect measurements based on simple commands that initiate special testing sequences which are stored in the system controller.

Fig. 3.a shows the protocol for data transfer between the data processing unit and the system controller for uploading and downloading data. A request is always initiated by the host followed by an acknowledge from the system controller and then command-specific functions are executed in the system controller. The transaction is completed by a data response that is generated when the command has been fully executed on the system's controller side. The data transfer protocol is implemented in the form of read/write commands, which are encapsulated in the TCP/IP packets. Fig. 3.b shows the format and the various fields of the command request, acknowledge and response.

Fig. 4 shows the NVM characterization platform with the different boards of the testbed including the AFE board with (2x) 14bit 60MS ADCs, (2x) 8bit 100MS ADCs, (7x) 12bit 100MS DACs, and (8x) SPI-based reference units, the two different FPGA boards, and a special chip support board tailored to a prototype NVM chip.

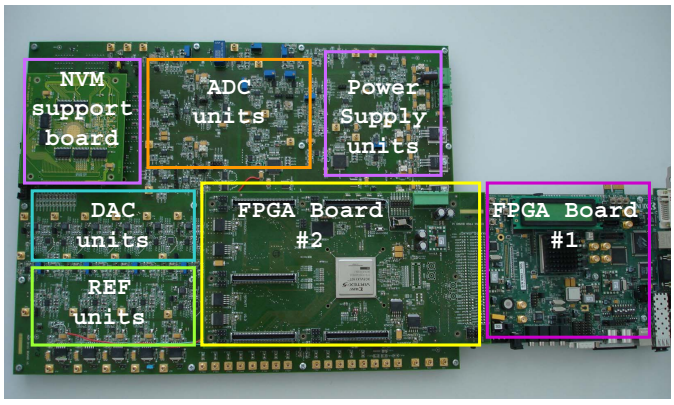

Fig. 4. Photo showing the NVM characterization platform.

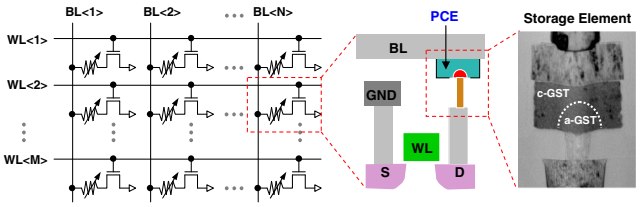

Fig. 5. Schematic of PCM test array organized in word-lines (WLs) and bit-lines (BLs) with NMOS FET selector device. Upon the application of a programming pulse, an amorphous GST (a-GST) region is generated within the crystalline GST (c-GST)volume close to the bottom electrode contact, thus changing the cell's electrical resistance.

III. Experimental Characterization of Non-Volatile Memories

This section presents experimental results of two different types of non-volatile memories, namely a prototype PCM chip and a commercial MLC Flash device, using the NVM testbed described in the previous section.

A. MLC Phase-Change Memory

Fig. 5 shows a schematic of the PCM array and cell architecture along with a cross-sectional tunnelling electron microscopy (TEM) image of the PCM cell based on $Ge_2Sb_2Te_5$ (GST). The PCM cells were integrated into a prototype chip serving as a characterization platform in 90 nm CMOS technology using the key-hole process described in [12]. In addition to the PCM cell array (2x2 Mcells), the memory chip contains the circuitry for cell addressing, read-out, and programming.

One of the attractive features of PCM is multi-bit operation which is achieved by effectively programming the memory cell into multiple resistance levels that correspond to different states of amorphous and poly-crystalline phase configurations [8]. The intermediate states span the resistance window between the full amorphous and the full crystalline sates, typically referred as RESET and SET states respectively. The programmable space is quantified by the characteristic programming curve which shows the change of the cell's resistance, or of the cell's read current at a given bias voltage, as a function of the programming current or voltage.

Fig. 6 shows an example of the characteristic programming curve of a PCM cell when rectangular programming pulses of increasing amplitude are used and the cell is initialized either to the RESET or the SET state by an appropriate RESET or SET pulse respectively. When initialization starts from the RESET state, a typical U-curve is obtained as the increasing programming current starts to crystallize the material until a minimum resistance value is achieved. Further increase of the programming current results in increasing the resistance as new amorphous material is generated by the melt-and-quench process [5]. The characteristic programming curve shows a resistance contrast of more than 2 orders of magnitude and a gradual increase between the lowest and the highest resistance with the programming current/voltage. These attractive features are exploited for multilevel programming where the

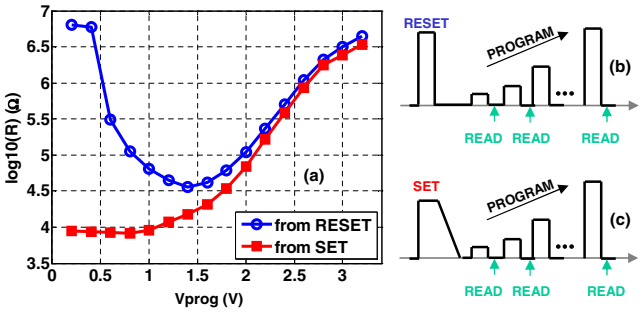

Fig. 6. (a) Programming curve of PCM cell after initialization of the memory cell to the (b) RESET or the (c) SET state.

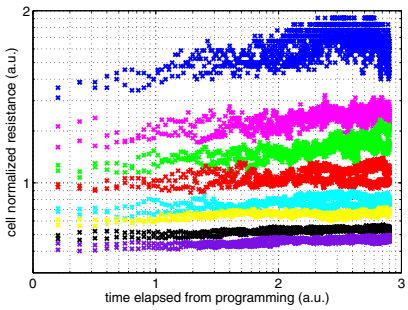

Fig. 7. Drift of multilevel resistance values in PCM as a function time. The higher the resistance of the cell-state, the larger the amorphous fraction, and thus the higher is the drift of the read-out signal.

cell is programmed in intermediate resistance levels between the RESET and SET states.

Due to cell variability issues which are typically observed in large cell arrays, an iterative programming scheme with feedback is usually employed for multilevel programming [13], [14]. The aim of the iterative algorithm is to adapt the programming pulse attributes, e.g., amplitude, width, trailing edge, in order to meet each cell's programming characteristics and at the same time ensure high convergence rate at low programming latency in terms of total programming iterations.

Experimental measurements of the read-out signal from cells programmed at different resistance levels can be effectively obtained by utilizing the data acquisition capabilities of the HW testbed. Such measurements can provide important information regarding the noise characteristics of the read-out signal as well as the retention of the programmed states over time. What is typically observed in phase-change materials is a temporal increase of the amorphous-phase resistivity, which is known as resistance drift. The resistance drift is modelled by the following empirical law $R(t)/R(t_0) = (t/t0)^v$, where $R(t)$ is the resistance measured at time t and v is the drift exponent [15]. Fig. 7 shows the change of the read-out signal expressed in cell resistance as a function of the measurement time that has elapsed from the time of programming the memory cell to the target resistance level. The various measurement plots correspond to different multilevel states and follow the above empirical power-law.

Studying the drift and noise characteristics of the PCM memory channel is crucial for the design and optimization of the programming and sensing schemes as well as for the developing of new signal processing and coding algorithms that are tailored to the characteristics of the device. Using the NVM testbed a systematic large-scale characterization study can be made in order to collect and analyze the statistics of the unique noise sources of the PCM memory channel. The noise and drift statistics can be used in order to build a powerful statistical channel simulator that provides a valuable tool for the evaluation of the device error-rate and retention performance [16]. The read noise in PCM is of low frequency nature and occasionally exhibits random telegraph signal steps of moderate amplitude, which may appear in all cell states, [17]. An accurate statistical channel simulator enables the

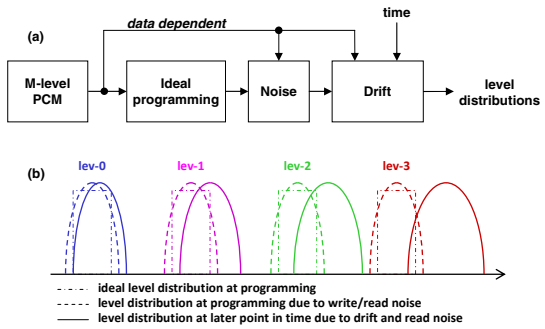

Fig. 8. Model for drift and noise disturbances of multilevel distributions in PCM: (a) model block diagram, (b) schematic description of change of ideal MLC distribution due to noise and drift.

estimation of the error probability of the memory array. Moreover, it allows the analysis of different level placement strategies. It is also possible to assess the MLC capacity of the array for a specific retention and BER target.

Fig. 8.a shows a graphical model that describes the various blocks of a statistical channel simulator that can be used to generate multilevel distributions based on characterization data from PCM devices. Fig. 8.b shows schematically the distortion of the level distributions in the 4-level PCM channel due to drift and noise. Ideally, 4 uniform level distributions are generated in the last verify step of the iterative programming scheme. Assuming perfect convergence, all distributions lie within the target level bins. However, due to noise in the write and verify process during programming, the distributions are no longer ideal and become of Gaussian type. Reading the stored information at later points in time, the level distributions will be further distorted due to drift and noise.

The NVM testbed provides a powerful environment for fast characterization and performance comparison of different devices in terms of material, process, cell and circuit design variations. Characterization of the multilevel PCM channel provides detailed insight into the different factors that distort the read-out signal and affect the reliability of the device. Moreover, it enables the design and evaluation of new signal processing and coding schemes that are tailored to the unique features of the PCM channel.

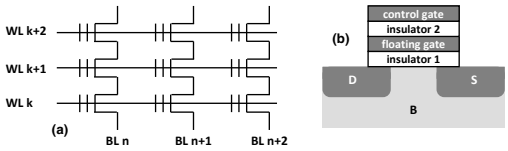

Fig. 9. (a) Basic diagram of NAND Flash array architecture and (b) schematic of Flash cell based on floating-gate MOS transistor.

B. MLC NAND Flash Memory

Flash memory is based on cells that use floating-gate transistors with two overlapping gates. Flash cells connected in series form blocks of pages and these devices are referred to as NAND Flash. Fig. 9 shows schematically the architecture of the NAND Flash array and the Flash memory cell based on the floating-gate MOS transistor [18]. Writing is allowed only after erasing a complete block of pages, while the lifetime and reliability of these devices are strongly related to the number of program/erase (P/E) cycles. MLC NAND Flash stores two bits per cell and results to higher densities, but wears out faster compared to single-level cell (SLC) NAND Flash.

When a solid state drive (SSD) is designed using MLC NAND Flash, it is important to characterize error rate performance of the Flash memory chips, since this will determine the proper design of line pre-coding and error control coding (ECC) schemes in order to achieve the target user BER for the lifetime of the device. The NVM testbed presented in this work can also be used for characterizing various prototype NAND Flash cell technologies as well as commercially available NAND Flash chips. In the latter case, special HW module modules are used in order to support a specific NAND digital I/O interface (i.e, ONFI, Toggle). The NAND Flash memories are loaded with various workloads and data patterns, in order to study their time-varying behavior and to collect information concerning the error conditions and response time, e.g, during page programming and block erasing. As the experimental results demonstrate in Fig. 10, the raw error-rate increases exponentially as a function of the P/E cycles.

IV. Conclusion

In this paper, we presented a high-performance HW testbed for experimental characterization and testing of solid-state memory technology. The testbed was build around a modular architecture based on reconfigurable FPGA-based HW modules along with a high-performance AFE. The platform consists a versatile prototyping environment, which enables the statistical characterization of the solid-state memory channel for new and emerging non-volatile memories with the goal to understand the noise and interference sources that affect the reliability of these devices. Experimental characterization results from PCM and Flash memory test devices have also been presented.

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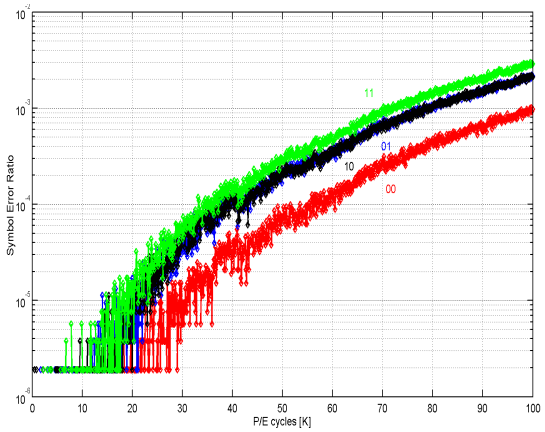

Fig. 10. Symbol error rate of MLC Flash device as a function of P/E cycles.

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