A Software-Radio Test-bed for Measuring the Performance of DVB-S2 Receiver Circuits

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***Abstract*—This paper presents a flexible and versatile DVB-S2 test-bed that combines a set of automated signal generation and analysis instruments along with a powerful software radio processing unit for executing performance analysis experiments of DVB-S2 receiver circuits using realistic scenarios. The test-bed provides a rich set of forward satellite channel impairments and also supports real DVB-S2 signals. All test-bed subunits are interconnected over a LAN and are controlled through a central processing unit, allowing fully automated data acquisition and processing of measurements collected from the various receiver circuits.**

I. Introduction

DVB-S2 comprises the newest European standard for broadband satellite communications that exploits new achievements in the fields of modulation and coding [1]. DVB-S2 meets the high performance requirements of today's satellite broadcasting and interactive communications, in terms of capacity and power efficiency, while keeping the complexity of the terminal receiver at acceptable levels. Both functional characteristics are based on the versatility of the DVB-S2 physical layer with frame-by-frame adaptability according to the channel conditions [2].

As a result of the DVB-S2 standardization, various products have been presented and new services are being launched by several broadcasters around the world. Verification of the DVB-S2 technology involves accurate signal measurements based on laboratory tests and product deployment under various transmission conditions. In particular, when commercial equipments are under test, accurate measurements are obtained using specialized instruments that emulate realistic signal impairments [3].

In this paper, we present a versatile test-bed for DVB-S2 signal measurements. The presented setup is based on a software radio platform that integrates a DVB-S2 digital receiver along with a custom data acquisition and control unit that allows the communication of the various receiver processing units with a high-level application for analyzing and presenting performance and diagnostic results and statistics. The test-bed can be used for measurements and analysis of DVB-S2 signals from an outdoor unit (ODU) as well as for signal validation and performance tests of commercial or prototype DVB-S2 receivers under fully controlled channel impairments.

The paper is organized as follows. Section II gives an overview of the test-bed architecture and its functionality. Section III describes the different subunits of the software radio processing platform that include the software radio receiver and its assisting subunits of measurement acquiring and GbE interfacing of the unit with the entire test-bed. Finally, Section IV summarizes the capabilities of the presented test-bed for emulating a wide range of noise sources typically encountered in forward satellite channels, while an example of symbol timing recovery performance measurement is presented.

II. DVB-S2 Measurement System

The DVB-S2 measurement system, presented in Fig. 1, consists of a versatile instrumentation environment based on commercially available equipment and custom devices that enable the measurement and analysis of a DVB-S2 receiver under different signal conditions and operating modes. The DVB-S2 measurement system consists of a set of DVB-S2 compliant signal generators, programmable up and down frequency conversion units, noise injection and multi-channel fading conditions emulator, a software radio based processing unit with signal demodulation and data acquisition capabilities and a host computing environment for visualization of measurements, diagnostics and signal statistics.

The basic DVB-S2 signal generator consists of a NEWTEC NTC2277 IF modulator at 70 MHz and an IP host traffic generator. System parameters like baud rate, modulation and coding modes, roll-off factor, Tx power are user controllable. DVB-S2 signal generation can also be performed by Vector Signal Generators under the control of a custom application that also determines the data traffic used in the transmitted XFECFRAMES.

The programmable frequency conversion unit (FCU) supports multiple signal paths, with independent L-band to IF and IF to L-band conversion modules, thus allowing the addition of various signal impairments at different signal processing stages. The FCU provides various signal distortion options, including white and colored Gaussian noise, RF interference, as well as non-linear effects using an SSPA power amplifier. Additionaly, the FCU can also be interfaced with an outdoor unit with a LNB that provides the received L-band signal.

The software radio processing unit (SRPU) consists of a digital DVB-S2 receiver with a data acquisition unit implemented on a reconfigurable hardware platform. The receiver performs signal demodulation and decoding according to [1],

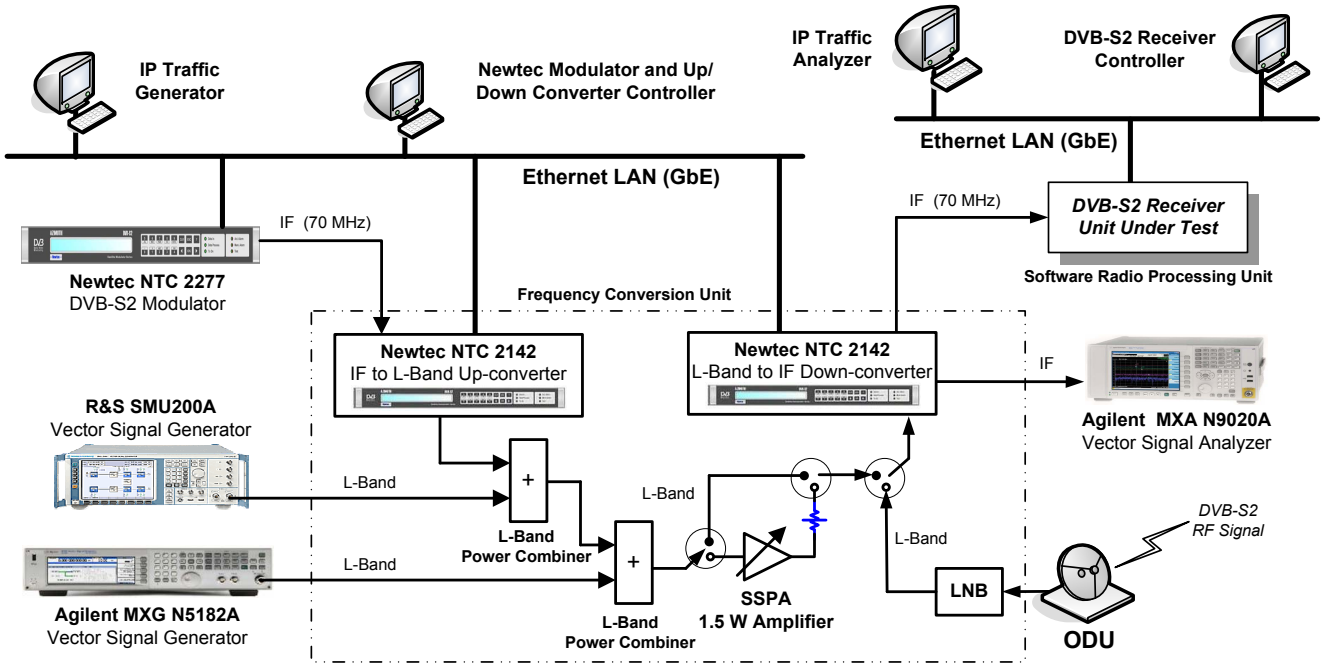

Fig. 1. The instrumentation and measurements setup.

while the data acquisition unit collects data from various stages of the signal processing chain. The hardware platform is based on a multi-processor environment that enables the functional mapping of the receiver circuits into multiple FPGA and DSP circuits, where additional resources are used for implementing multi-domain signal processing and data acquisition functions. For real-time operation, the inter-communication between the various modules is based on high-speed data channels, while the DSP firmware is based on priority-based task scheduling.

The host computing environment provides data processing and visualization, generates measurement reports and performance statistics based on a high-level custom application using the MATLAB environment. The interconnection and control between the various measurement units is realized via a Gigabit Ethernet (GbE) link. The setup also uses high-precision commercial instruments, such as Vector Signal Generators for noise injection and a Vector Signal Analyzer for general purpose signal measurements at the input of the SRPU. All instrumentation components are controlled by the host computing environment.

III. Software Radio Processing Unit Description

The software radio processing unit (SRPU) comprises the basic unit of the presented test-bed, since it performs all the necessary signal processing and measurement of the DVB-S2 transmission parameters. It consists of a complete DVB-S2 IF digital receiver [4] and a multi-domain data acquisition module for signal measurements and diagnostic reports. Furthermore, a controller subunit is used for maintenance and monitoring the SRPU operation, while a LAN is used for data exchange and control. The architecture and the functional structure of the SRPU is given in Fig. 2, where the DVB-S2 signal flow and data interconnections between the different submodules are depicted.

A. DVB-S2 IF Digital Receiver

The digital receiver is the main unit of the SRPU. The analog IF input (70MHz), that is derived from an external L-IF frequency converter (L-IF FC), is digitized by an intermediate-speed and high resolution analog to digital converter (ADC). The gain of the frequency converter determines the signal's output level and is controlled by a custom power control subunit, which properly adjusts the FC gain according to the dynamic range of the ADC. This operation is based on power measurements using the ADC samples, while gain adjustment is performed over the LAN, using data exchange between the SRPU and the external L-IF FC.

The ADC samples are fed to the first signal processing subunit, which is the digital down-converter (DDC) [5], which converts the real IF signal into the respective baseband one, by using two cascaded stages of frequency conversion. The first stage mixes the input signal samples with a quadrature oscillator of a fixed frequency. Then, the resulting signal feeds a programmable frequency converter stage that utilizes a numerical control oscillator (NCO). The NCO frequency is controlled by the decisions of the coarse carrier frequency recovery (CFR) subunit described later. At the output of the second frequency conversion stage, a sample rate conversion takes place that aims of producing the necessary rational rate change factor, so that the sampling rate at the DDC output is adjusted to an integer multiple of the nominal symbol rate.

At the next processing stage, the signal's symbol rate is estimated and recovered by using a mechanism that tracks the

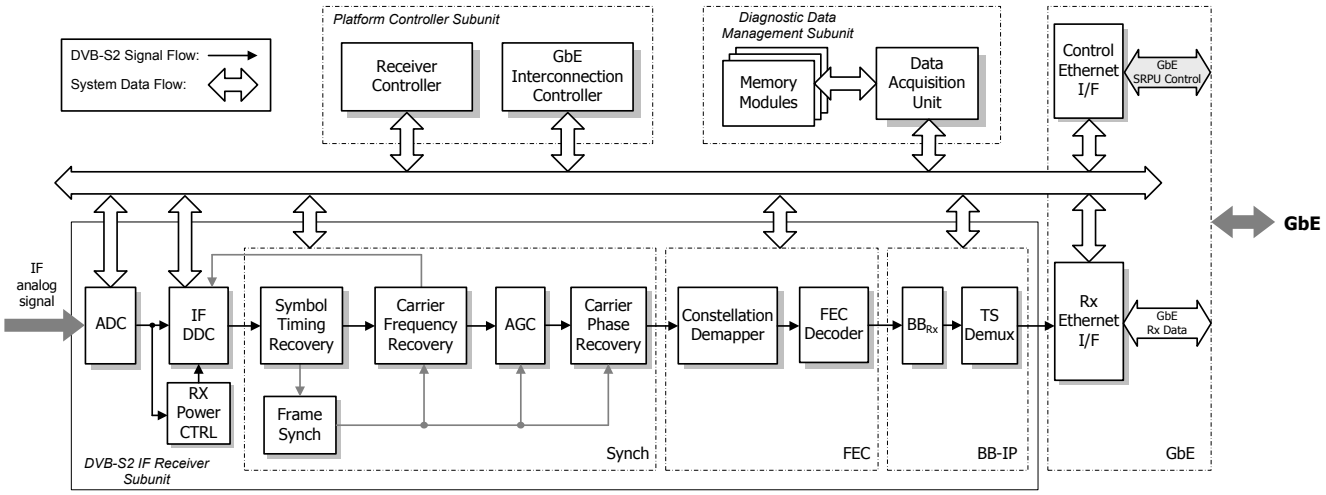

Fig. 2. Software radio unit functional architecture.

symbol rate fluctuations introduced during the signal transmission and generates the synchronized samples to the incoming symbols. Symbol timing recovery (STR) is implemented as a second order feedback loop utilizing a Farrow structured interpolator along with the non-data-aided (NDA) timing error detector (TED) proposed by Gardner [6]. Gardner TED is capable of operating under random symbols and unknown carrier frequency offset error without the need of precise carrier synchronization. Then the synchronized stream of samples is matched filtered and downsampled leading to a rate of one sample per symbol, which feeds the next receiver processing stage, the frame synchronizer. As soon as STR is achieved the boundaries of the DVB-S2 physical layer (PL) frames are detected. This is done by searching the position of the physical layer header using an appropriate correlator. Using differential detection, accurate frame synchronization is possible even in the presence of strong carrier frequency errors [7], [8]. Based on the correct framing alignment, it is possible to demultiplex the pilot symbols from the incoming frame in order to feed the various pilot-aided carrier and phase synchronization subunits.

Carrier frequency recovery is invoked directly after the frame synchronizer has detected the start of the transmitted frames and thus the locations of the pilot fields. The recovery is performed in two sequential steps, which both use the known pilot symbols. The first step of carrier synchronization consists of a coarse carrier frequency (CFR) recovery mechanism which compensates large frequency offset errors up to several MHz and is implemented as a second order feedback loop, based on a delay-and-multiply (DM) frequency error detector [9]. The compensation of this loop is applied through the NCO that is implemented in the DDC. The second step completes the carrier synchronization process, since it performs fine carrier frequency recovery (FFR) that is initiated after the convergence of the first carrier recovery loop, where the frequency offset error is in the order of a few hundreds of kHz. Fine recovery deploys a feedforward estimation algorithm, derived from an alteration of the L&R technique [10].

The resulting residual frequency offset is compensated by using two phase recovery mechanisms. In case of low order modulation transmissions (QPSK or 8PSK), a pilot-assisted maximum-likelihood (ML) feedforward estimator is used for computing the average phase of each pilot field [9]. Accordingly, phase compensation is based on the interpolation between the estimations of two consecutive pilot fields, for determining the evolution of the phase during the transmission of intermediate data symbols. When high order modulations of 16 or 32 APSK are used, an additional phase synchronizer (fine phase recovery-FPR) is needed which consists of a closed loop based on the NDA phase error detector of Q-th power (Q=3 for 16APSK and Q=4 for 32APSK) [7]. Between these two procedures a digital automatic gain control (DAGC) takes place, which is based on a data-aided vector tracker mechanism (DA-VT) [11], which utilizes the known pilot symbols for the determination of the amplitude normalization multiplication factor. All the above procedures are performed into the *SYNC* receiver submodule.

Finally, the retrieved symbol stream is forwarded to the signal constellation demapper and the respective bit frames are further processed by the forward error correction (FEC) submodule (*FEC*) that incorporates LDPC and BCH decoding with interleaving. The generated LDPC/BCH decoded frames are processed by the respective submodule (*BB_IP*) in order for the IP datagrams to be extracted and forwarded to the GbE Ethernet network.

B. Control and Diagnostic Data Management Subunits

The diagnostic data management subunit is responsible for capturing and storing debugging information and performance parameters from the various stages of the DVB-S2 receiver and associates them to a common time-scale. The collected data are related with the I/Q quadrature signal components and the recovered bitstreams. This subunit also collects parameters from various receiver stages that are related either to the synchronization (*SYNC*) or the decoder (*FEC*). Such

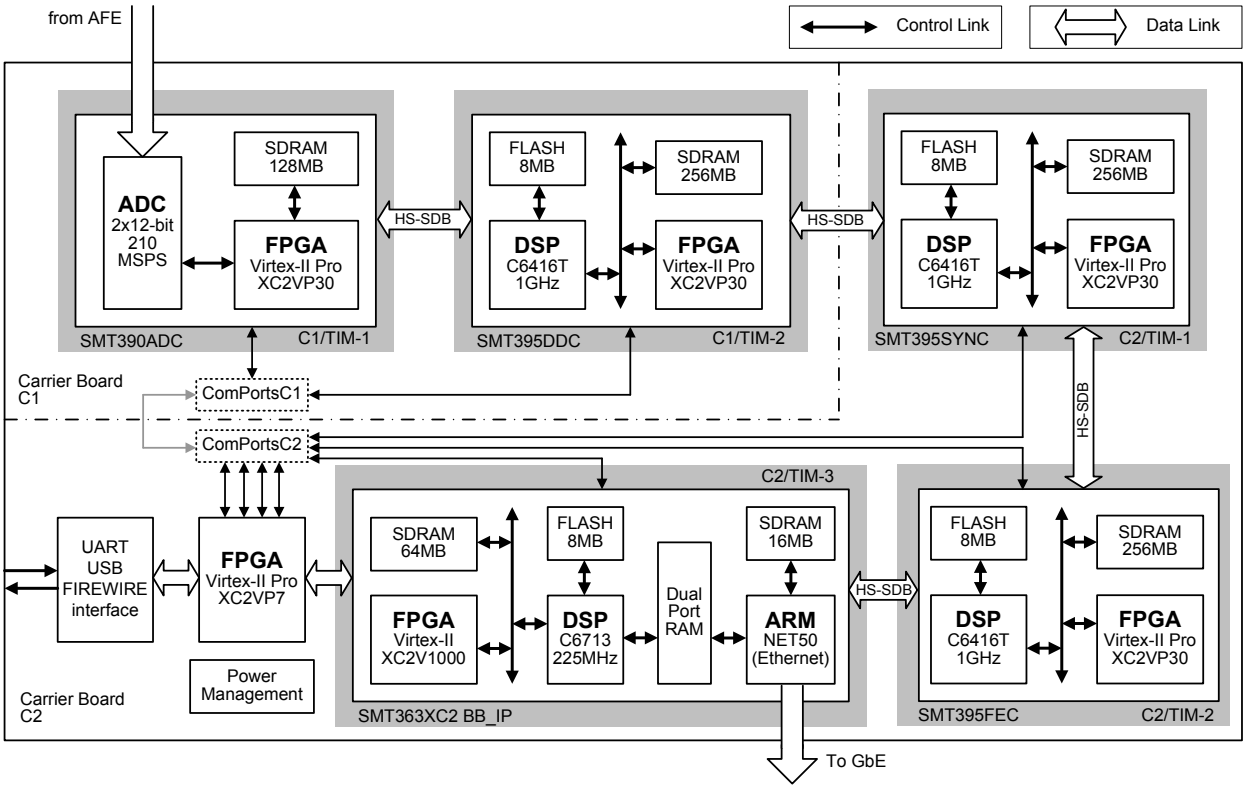

Fig. 3. The hardware platform of the SDR test-bed.

parameters include estimated symbol rate, carrier frequency and phase and I/Q signals.

The operation of the DVB-S2 receiver, the data acquisition process and the uploading of measurements data are controlled by the controller subunit. The platform controller is also responsible for configuring the various receiver submodules (e.g. to set-up the correct coding rate, modulation, frame size, nominal symbol rate, roll-off factor), as well as for programming the data acquisition unit to capture specific signals for analysis and visualization.

All of these procedures are initiated by a high-level GUI application running on the central processing unit, where post-processing and visualization is performed using MATLAB environment. Based on the presented measurement system architecture, we are able to fully analyze a DVB-S2 signal as well as to observe the evolution of several signal parameters at the various stages of the DVB-S2 receiver. By combining these measurements, from the synchronization and decoding subunits, we are also capable of validating the performance of their circuits, while having a better understanding of the effect of various channel conditions to receiver performance.

C. Hardware Platform Architecture

The implementation of the DVB-S2 digital IF receiver, along with its additional logic for parameter acquisition and control, is based on a versatile and powerful hardware prototyping platform based on multiple DSPs and FPGA circuits. The prototyping platform, which is shown in Fig. 3, consists of two carrier boards (C1 and C2) by Sundance which incorporate five Texas Instruments Modules (TIM). The carrier boards provide all the necessary physical connections between the different TIMs, while they use a Virtex-II Pro (XC2VP7) device, that incorporates a PowerPC processor, for management and control purposes.

TIM-1 of the first carrier board C1 is used to digitize and process the incoming IF signal by an intermediate-speed 12-bit ADC (up to 210 MSps) and a Virtex-II Pro (XC2VP30) FPGA with a PowerPC processor. An SDRAM of 128MB is also available for storage purposes. TIM-2 of C1 combines a powerful C6416T DSP running at 1GHz and a Virtex-II Pro (XC2VP30) FPGA. Due to the high performance DSP, the TIM-2 module is used for implementing the Digital Down Conversion (DDC) of the DVB-S2 receiver. At the other carrier board, TIM-1 also incorporates an other C6416T DSP and a Virtex-II Pro (XC2VP30) FPGA suitable for the implementation of demanding designs, such as synchronization procedures. C2/TIM-2 utilizes the same hardware as the previous TIMs for implementing the FEC receiver submodule, while the C2/TIM-3 combines a C6713 DSP running at 225 MHz, a Virtex-II FPGA and a NetSilicon ARM-chip with an Ethernet MAC controller. The above hardware platform provides the necessary flexibility to adapt the functionality of the receiver logic to various platform circuits and also the required extra resources, such as memory modules and processing power for the additional acquisition and monitoring mechanisms.

TABLE I
SYMBOL RATES VERSUS PROCESSING RATES AT VARIOUS RECEIVER SUBMODULES.

R_s (MBaud)	ADC (MSps)	IF-DDC (MSps)	Symbol Timing (MSps)	Frame/Carrier/Phase Recovery (MSps)
10.0	200	40	20	10.0
12.5	200	50	25	12.5
15.0	180	60	30	15.0
17.5	210	70	35	17.5
20.0	200	80	40	20.0
22.5	180	90	45	22.5
25.0	200	100	50	25.0

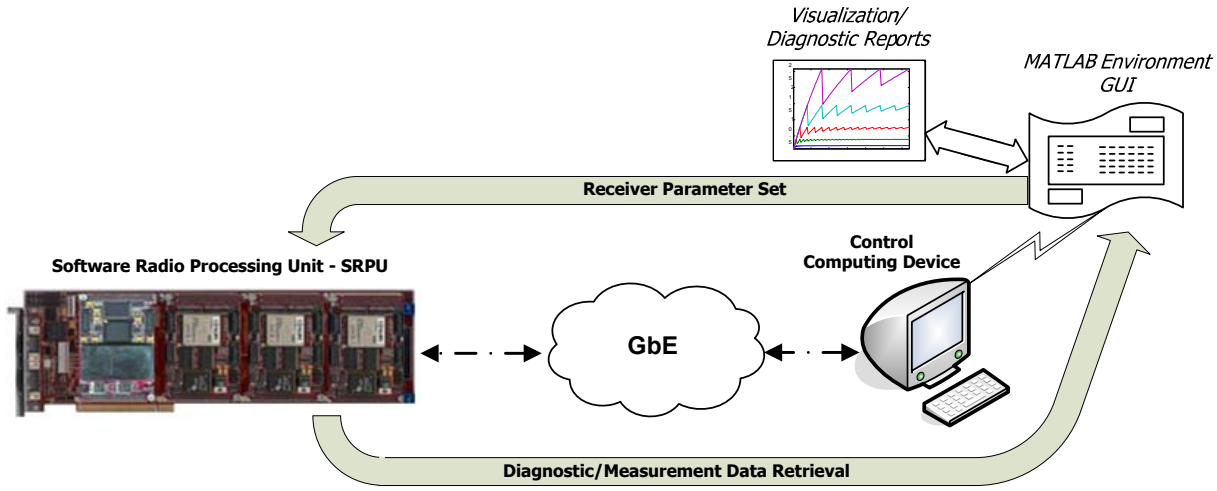

Fig. 4. Data exchange procedures between SRPU and the central processing unit.

D. Functional Mapping and Complexity

According to the receiver functional description in subsection III-A and the available resources depicted in Fig. 3, the mapping of the various receiver subunits is performed as described below. The C1/TIM-1 (SMT390ADC) is responsible for digitizing the analog IF signal and feeding the next processing unit with the pre-processed ADC samples. The control of ADC circuits and the management of samples in order to be transferred to the next TIM is totally performed in the reconfigurable logic of the available FPGA. At the other end, the FPGA and the DSP of the C1/TIM-2 (SMT395DDC) implement the Digital Down Conversion functions.

Synchronization functions are performed in the DSP of C2/TIM-1 (SMT395SYNC) at the second carrier board, which includes the STR module, the matched filter, the frame synchronizer, the carrier frequency and phase recovery and finally the amplitude control. The demapper, which retrieves and organizes the blocks of the coded bits, is implemented in the DSP of C2/TIM-2 (SMT395FEC) along with the deinterleaving and LDPC/BCH decoding. The last TIM C2/TIM-3 (SMT363 BB_IP) module is used for protocol processing (ULE, MPE and Data Piping) and the decapsulation functions, along with the required TCP-UDP/IP protocol stack, which forwards the received DVB-S2 data to GbE interface. Apart from the above functions, the last TIM is also responsible for processing the control commands of the central processing unit. The commands are executed locally by the TIM C2/TIM-2 controller and are realized as a set of DSP tasks running on the signal processors of all platform TIMs. These tasks are related with the parameters setting at the various receiver submodules and with the collection of diagnostic data and performance measurements. FPGA logic of all TIMs is responsible for realizing the DVB-S2 signal flow data transfers. Additionally, reprogrammable logic is used for implementing the control links between the TIMs.

Table I presents some representative symbol rates (R_s) and the respective processing rates at several receiver submodules of the hardware platform. These values correspond to a bandpass bandwidth of 36 MHz at the external L-IF frequency converter, a carrier IF frequency of 70 MHz, a maximum A/D converter sampling rate of 210 MSps and a roll-off factor 0.35. The sampling rate values have been selected in order to satisfy the Nyquist criterion as well as the DDC implementation [5].

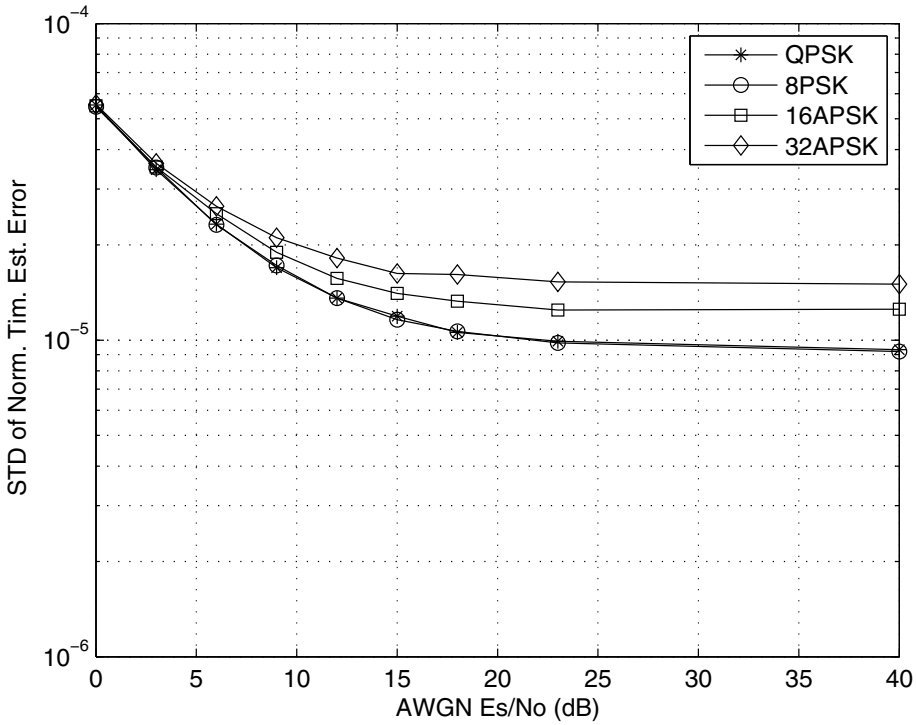

Fig. 5. STR performance in AWGN in terms of STD of the normalized timing estimation error $(\tau - \hat{\tau})$/T.

The presented test-bed also supports a parameters and diagnostics data exchange procedure, which is based on a high level application, running at the MATLAB environment of the central processing unit (control computing device) and at the processing tasks running on the various TIMs, under the coordination of the tasks of C2/TIM-3 (SMT363 BB_IP). As it is shown in Fig. 2, the high level application sends requests/commands in the form of TCP/IP packets. Two types of commands are supported and are served by the two controller submodules, as it is shown in Fig. 2. Both controller submodules are implemented as a set of interconnected DSP codes running on all available processors of the hardware platform. The commands either set the receiver's parameters or retrieve measurement and diagnostic data from the various receiver submodules.

IV. DVB-S2 Signal Validation: The Symbol Timing Recovery Performance Case

The test-bed shown in Fig. 1 was also used for measuring the performance and for conformance testing of a custom DVB-S2 receiver under various channel impairments. DVB-S2 reference signal generation is based either on a DVB-S2 compliant IF modulator or a powerful RF Vector Signal Generator. Several types of impairments can be induced into the transmitted signal either at the IF or the L-Band:

- Additive white Gaussian noise (AWGN).
- Fading conditions (Standard/Fine Delay, Pure Doppler, Rayleigh, Rice, Lognormal and Suzuki).
- IQ Impairments (offset, gain imbalance, quadrature offset).
- Carrier frequency offset errors.
- Symbol rate offset errors.
- Any combination of the above.

A significant channel impairment that is supported by the test-bed is the non-linear amplification behavior typically encountered in the transponder of the forward satellite channel, by using an SSPA amplifier. According to the amplifier's AM/AM characteristics, we are able to evaluate and determine the performance of the various processing stages of the device under test under the specific conditions.

As an example, in Figure 5 we present performance measurements of the symbol timing recovery (STR) submodule of the SRPU under AWGN conditions, derived using the above mentioned test-bed. The measurement results have been derived according to the following procedure: The control computing device sets the SRPU parameters during initialization. Then the data that have to be collected are defined (the loop filter output in this case). Then, the signal generation modules are programmed, the receiver is started and when the STR loop converges to the actual symbol rate, the collected data are stored at the memory of C2/TIM-1. Finally, the high-level application receives the collected data. The above procedure is performed for all different AWGN levels in order for the STR loop performance to be measured.

V. Conclusions

In this work the architecture of a software radio test-bed that can be used for measuring the performance of various DVB-S2 receiver circuits has been presented. The various units of the test-bed have been analyzed functionally. The presented test-bed comprises a fully control environment for realizing testing and measurement procedures that provide a clearer insight to the overall receiver performance under realistic channel conditions.

Acknowledgments

This work was supported by the European Regional Development Fund (ERDF) and the Greek Ministry of Development - General Secretariat for Research and Technology (GSRT) in the framework of project 'AKMON'.

The authors would like to give special thanks and appreciation to A. Kotsopoulos, M. Varsamou, C. Stavroulopoulos and E. Zacharias for their invaluable contributions to the system prototyping effort.

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